Analysis of Switching Noise on Power Planes

Mirjana Ž. Stojilović and Antonije R. Djordjević

Abstract — **Power delivery networks (PDNs) in modern printed circuit boards (PCBs) are usually realized using power planes. Since the planes have very low inductance, it is usually believed that such PDNs have the smallest amount of switching noise. However, in reality, the power planes can resonate. The noise at resonant frequencies can be significant and it deteriorates the PDN performance. One of the classical methods for decreasing the noise is bypassing. This paper investigates the behavior of a typical PDN and the effect that real SMD bypass capacitors produce when attached to it.**

Keywords —**Power-delivery networks, switching noise.**

I. Introduction

POWER-DELIVERY networks serve to distribute power to all devices in a digital system, and to provide stable voltage references for digital signals [1]. These networks consist of power and ground wirings. When designing them, it is important to provide low-impedance connections to all power and ground pins of integrated circuits (ICs). This is usually done by using solid power planes, separated by a thin dielectric layer. These planes have remarkably low inductance. Besides that, they share a lot of mutual capacitance that provides a low-impedance path between power and ground pins at very high frequencies. Discrete bypass capacitors are usually added to help reduce the impedance at lower frequencies. The major problem with the power planes is that they exhibit multiple resonances [1], [2]. The bypass capacitors are usually arranged in banks and altogether also exhibit their own multiple resonances. These resonances should be suppressed by proper damping of the structure.

In this paper we present performance analysis of a typical PDN made of two solid power planes, when the connected ICs switch their states. Induced voltage variations between the planes represent noise that is known as the simultaneous-switching noise. Although the analysis is performed on a simplified PDN model when only one IC induces the noise, the results and conclusions obtained can be applied to more general cases. We also investigate effects produced by attaching real SMD bypass capacitors to the PDN. The present paper is inspired by the pioneering research on the power-plane resonances [2], where a wire-grid model of the planes was used. We upgrade [2] by building a more sophisticated model using program [3]. We also experimentally verify the simulation results.

In section II we introduce the model of the PDN along with components of the digital system attached to it. We also present relations between voltages and currents at certain points (ports) of the structure. Those relations are used later to find voltage waveforms at the ports. In section III we present and compare simulated and measured results for the impedance parameters of the PDN. In section IV we explain computations of the port voltages. In section V a typical bypass capacitor is assumed to be attached to the PDN, and its effect on the PDN performance is analyzed.

II. Power-delivery network model

A simplified model used for measurement and analysis consists of a pair of planes of dimensions 120 mm by 180 mm with dielectric FR-4 that fills the space between the planes. The separation between the planes is 0.6 mm. Five locations for connecting power-delivery network elements (i.e., power supply and ICs) are chosen on the planes. Their coordinates will be given later. At each location we have one port, so the whole PDN structure can be regarded as a five-port network.

This network is assumed to represent a power-delivery system for four ICs. The stabilized power supply is modeled by an ideal voltage generator in series with a small resistance, $R_0 = 0.1\,\Omega$. We assume that the power supply is connected at port s ($s = 5$), and that the four ICs are connected at the remaining ports. In the quiescent state, all ICs drain constant currents, so the voltage between the planes is constant. However, this is not the case when ICs switch their states. For simplicity, we will calculate voltage variations induced when only one IC switches its state.

For example, let the logic circuitry inside the IC connected to port p ($p = 1$) switch from one logic state to another. While this is happening, the current through the power pins of this IC exhibits a sharp transient, but the remaining ICs still drain constant currents. We are interested only in finding the voltage variations between the planes. Since the d.c. voltage in the steady state is identical for all ports, we can exclude it from calculations. Hence, port $s = 5$ remains terminated only by the resistance R_0. For the transients, ports 2, 3, and 4 behave as if they are open, and port $p = 1$ behaves as if it is driven by a current generator that models the variations of the current. The resulting equivalent scheme is presented in Fig. 1.

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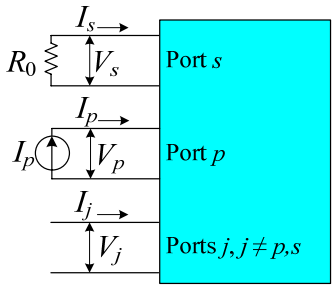

Fig. 1. PDN as five-port network.

Generally, for a multiport structure (with $P = 5$ ports in our case), the port voltages and currents are related in the frequency domain as

$$[V] = [z][I], \tag{1}$$

where $[V]$ is a column matrix containing the port voltages, $[V] = [V_1,...,V_P]^T$ (T denotes transpose), $[I]$ is a column matrix containing the port currents, $[I] = [I_1,...,I_P]^T$, and $[z]$ is a square matrix of the impedance parameters,

$$[z] = \begin{bmatrix} z_{11} & \cdots & z_{1P} \\ \vdots & \ddots & \vdots \\ z_{P1} & \cdots & z_{PP} \end{bmatrix}. \tag{2}$$

In the considered PDN system (Fig. 1), the current at port $p = 1$ is assumed to be known (I_p). The voltage and current at port $s = 5$ are related as

$$V_s = -R_0 I_s . \tag{3}$$

The currents at all other ports are zero.

In order to find the transient voltages, we first evaluate the impedance parameters of the PDN, as a function of frequency. Then, we assume the time-domain waveform of the current transient i_p and use FFT to find its samples in the frequency domain. Thereafter we find the port voltages in the frequency domain using relations (1) and (3). Finally, we use the inverse FFT to find the corresponding waveforms of the port voltages.

III. Impedance Parameters

A. Simulation

The goal of the simulation is to find the impedance parameters of the considered five-port PDN. The simulation is performed using WIPL-D Microwave software [3]. This software can be used for fast and accurate simulation and design of microwave circuits, devices, and antennas. Its 3D electromagnetic (EM) solver is a frequency-domain solver based on the method of moments [4].

The simulation model is shown in Fig. 2. Connections to the two planes are modeled as short wires that interconnect the planes. Those wires are labeled w1 through w5. Each wire carries a port. The (*x*,*y*) coordinates of the ports are P1 (30, 20), P2 (150, 20), P3 (90, 60), P4 (30, 100), and P5 (150, 100). All coordinates are in mm.

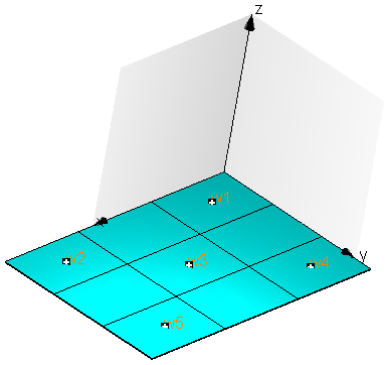

Fig. 2. Simulation model.

The space between the planes is filled with dielectric FR-4. Its permittivity is frequency dependent [5] and varies from sample to sample. In order to get precise simulation results while using a simplified approximation, we choose the following complex permittivity:

$$\varepsilon_r = \varepsilon' - \mathrm{j}\varepsilon'' = 4.33 - \mathrm{j}\,0.0866 . \tag{4}$$

The real part of the permittivity ($\varepsilon' = 4.33$) provides the best fit with our experimental data, and the imaginary part ($\varepsilon'' = 0.0866$) corresponds to the common value of the loss tangent ($\tan\delta = 0.02$). Conductive losses are also included in the simulation model by setting the metallization conductivity to $\sigma = 50$ MS/m.

The simulation is performed for 200 frequencies that are uniformly distributed in the range from 15 MHz to 3000 GHz (the separation between adjacent frequencies is $\Delta f = 15$ MHz). The simulation results are the impedance parameters of the PDN structure.

Due to the inherent symmetry of the $[z]$ matrix that is a consequence of reciprocity, as well as the symmetry of the PDN structure, out of 25 impedance parameters, there are only five distinct values: $z_{11} = z_{22} = z_{44} = z_{55}$, $z_{12} = z_{21} = z_{14} = z_{41} = z_{25} = z_{52} = z_{45} = z_{54}$, z_{33}, $z_{13} = z_{31} = z_{23} = z_{32} = z_{34} = z_{43} = z_{35} = z_{53}$, and $z_{15} = z_{51} = z_{24} = z_{42}$.

In Fig. 3 and 4, the real (red line) and imaginary (blue line) parts of the impedance parameters z_{11} and z_{12} are plotted as a function of frequency. The diagrams for other impedance parameters are similar. Besides the simulation results, Figs. 3 and 4 also show the experimental results. The peaks in these figures correspond to resonances of the PDN structure.

B. Measurements

Laboratory measurements are performed on a double-sided printed-circuit board whose dimensions match the dimensions of the simulation model (width, length, and separation between the planes). The dielectric between the planes is FR-4. The ports are realized using SMA connectors. Measurements of the impedance parameters are done using the network analyzer Agilent 5062A. In order to achieve good measurement results, calibration and reference plane adjustment are performed. The reference plane adjustment is necessary because the reference plane for network analyzer is in the middle of its SMA

connector, but in WIPL-D Microwave simulation software, the reference plane is on the surface of the ground plane. This adjustment is done by adding a delay in the calibration settings of the analyzer. The delay depends on the length of the SMA connector and the permittivity of its dielectric.

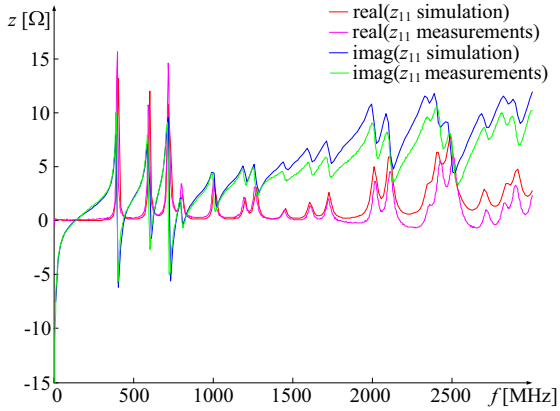

Fig. 3. Simulation and measurement results for real and imaginary parts of z_{11}.

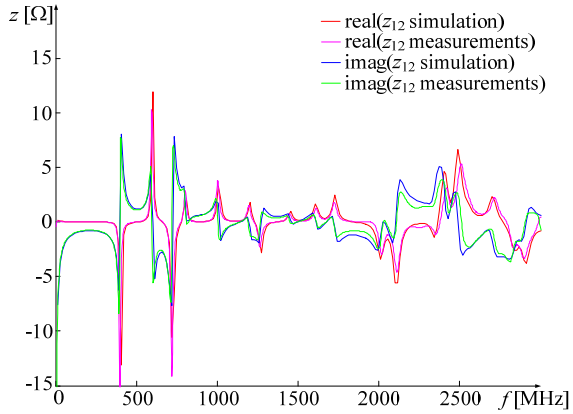

Fig. 4. Simulation and measurement results for real and imaginary parts of z_{12}.

The real and imaginary parts of the measured z_{11} and z_{12} parameters are plotted along with simulation results in Fig. 3 and 4. Obviously, the experimental results are in very good agreement with the simulation results.

IV. Calculations in MATLAB

A. Current Transient Waveform

Modern ICs work with clock frequencies that range from few hundred MHz to few GHz, depending on the application. Here we assume that the logic inside the IC connected to the port $p = 1$ switches the state with frequency of few hundred MHz and that the current transient lasts about $1\,\text{ns}$. The waveform of the transient i_p is assumed to be a pulse, with rising and falling edges having a squared-cosine form as in Fig. 5.

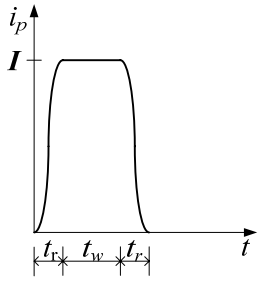

Fig. 5. The waveform of the current transient i_p.

We assume that the rise and fall times of the pulse are $t_r = 250\text{ps}$, the duration of the pulse flat part is $t_w = 750\text{ps}$, and the pulse amplitude is $I = 1\,\text{A}$. We Fourier transform the waveform using $N = 2^9 = 512$ samples (corresponding to the sampling frequency $f_S = N\Delta f = 7.68\,\text{GHz}$). The results obtained are samples in the frequency domain, $I_p(f_0)$, $I_p(f_1)$, ..., $I_p(f_{511})$, where $I_p(f_0)$ is the d.c. component of the current transient.

B. Port Voltage Waveforms

For the transient, the d.c. components of the port voltages are $R_0 I_p(f_0)$. Since we computed the impedance parameters at 200 frequency points, the samples $I_p(f_{201}) \div I_p(f_{255})$ are assumed to be zero. For each frequency, the samples of port voltages are calculated using relations (1) and (3). The port voltages obtained in the frequency domain are then transformed to obtain the time-domain waveforms. Two calculations are performed: one using the simulated data and another using the experimental impedance parameters.

The voltage variations at port $p = 1$ (waveform v_1) are presented in Fig. 6. The waveform obtained using the simulated impedance parameters (red line) shows very good agreement with the waveform obtained using the experimental impedance parameters (blue line).

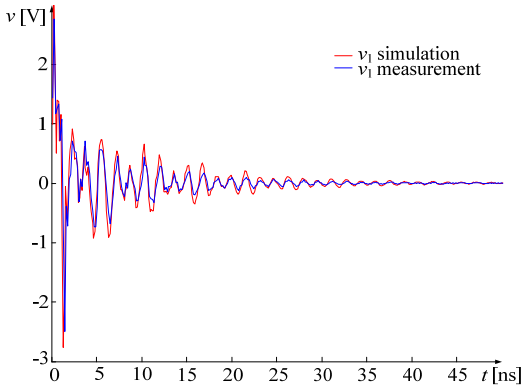

Fig. 6. Transient voltage waveforms at port $p = 1$, obtained using simulated and experimental data.

The current transient at port $p = 1$ causes oscillations in all port voltages because of the PDN resonances. At some ports, the peaks of the voltage variations are larger than $1\,\text{V}$. Since the power supply voltages for modern ICs are not higher than only a few volts, these variations can

present a serious problem and result in IC malfunction. The largest peaks are at port $p=1$ where the current transient occurs.

V. Bypassing

A. Bypass Capacitor Resonant Frequency

One common way to improve the PDN performance is to connect bypass capacitor groups in parallel with power and ground pins of the ICs, and close to them. Their purpose is to provide low-impedance paths between power and ground pins at medium and low frequencies. Besides the capacitance (C), real SMD capacitors exhibit parasitic series resistance (R) and series inductance (L). The inductance interacts with the capacitance of the capacitor, causing it to resonate at frequency

$$f_{\text{res}} = \frac{1}{2\pi\sqrt{LC}}. \tag{5}$$

For frequencies above f_{res} the inductive behavior of the capacitor dominates. Besides this resonance, there are resonances due to the presence of capacitor banks and the interaction between the capacitors and the planes. By adding the capacitors, the resonant frequencies of the PDN will be changed, but not suppressed. If we assume that the planes behave as a lumped capacitor C_p, the new resonant frequency will be:

$$f_{\text{res}} = \frac{1}{2\pi\sqrt{L\dfrac{C_p C}{C_p + C}}}. \tag{6}$$

Hence, real capacitors can only help to shift the resonances out of the IC's operating frequency band. Suppressing resonances can be done by adding resistors for dissipating noise energy [2], [6].

B. The Effects of C, R, and L on PDN Performance

The capacitive, resistive and inductive components of real SMD capacitors produce different effects on the PDN performance. In order to analyze them, we assume that those components are connected in series and attached at port $p=4$. In the frequency domain, the voltage and current at this port are now related by $V_4 = -Z_4 I_4$, where Z_4 is the impedance of the real capacitor. Fig. 7 shows voltage variations at ports $p=4$ and $p=3$ when port $p=4$ is open (yellow line) and when the following components are attached to it: one ideal capacitor $C=100\,\text{nF}$, one ideal inductor $L=1\,\text{nH}$ in series with C, one ideal resistor $R=3\,\Omega$ in series with C, and all three elements in series. The capacitor alone suppresses the noise at port $p=4$ (green line), but it does not suppress the noise at port $p=3$. (To effectively reduce the noise at port $p=3$, a low-inductance bypass capacitor should be attached to that port too.) Obviously, even the small parasitic inductance of $1\,\text{nH}$ substantially impairs the capacitor effect (blue line). A resistor connected in series with C helps in reducing the oscillations (red line). In order to achieve a notable effect, the resistance must be much greater than the typical parasitic resistance of the SMD capacitors. Hence, in practice, an SMD resistor should be attached in series with the bypass capacitor. The simulation showed that the best result can be achieved using the resistance of about $R=3\,\Omega$. The parasitic inductance of $1\,\text{nH}$ slightly reduces the effect of the resistance.

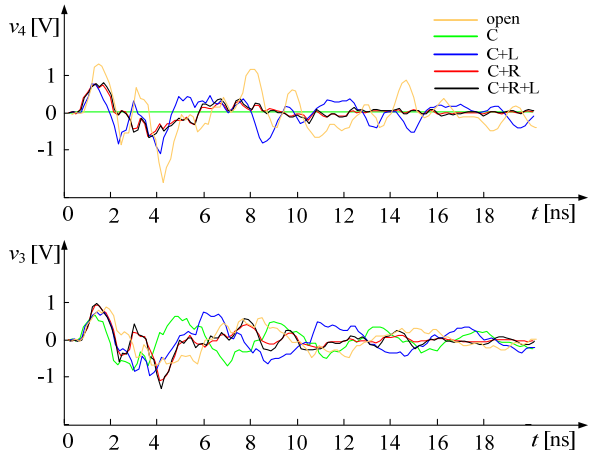

Fig. 7. Voltage waveforms at ports $p=4$ and $p=3$ for various terminations at port $p=4$.

VI. Conclusion

The power planes exhibit switching noise, in particular at resonant frequencies. SMD bypass capacitors are believed to effectively suppress the noise. However, their performance is deteriorated by the parasitic inductances of vias and the SMD components. These inductances can be lowered by utilizing special SMD capacitors and/or by embedding the capacitors into the PCB.

The resonances of the power planes can be suppressed by deliberately increasing the losses in the capacitors, e.g., by inserting series resistors. These resistors only act at high frequencies and they do not contribute to the d.c. power dissipation.

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