On-Wafer Measurements for Extraction of Effective Dielectric Constant in IC Transmission Lines on Multilayer Substrates

Radosvet G. Arnaudov, *Member, IEEE,* and Radoslav B. Borisov, *Member, IEEE*

***Abstract* — Methodology for extracting an effective dielectric constant of microstrip transmission lines on multilayer substrates, from measured or simulated S-parameters data, using on-chip test structures, has been demonstrated. The methodology consists of: 1) building on-chip interconnect structures usually implemented in calibration and de-embedding procedures in microwave on-wafer test and measurements – transmission lines, stubs and pad launchers; 2) extracting the effective dielectric constant from the characteristic impedance and propagation constant of these structures, fully described by the measured or EM-simulated S-parameters. The demonstrated methodology is applicable for evaluation of dielectric and semiconductor multilayer substrates, both with lossy and lossless characteristics over a broad frequency band. Another advantage is implementation of very short transmission line structures with physical dimensions much smaller than a quarter wavelength of the highest investigated band frequency, thus preserving a valuable chip area in the test structures and being compatible with some of the calibration TRL elements.**

***Keywords* — Calibration and de-embedding structures, characteristic impedance, effective dielectric constant, multilayer substrates, on-wafer test and measurements, propagation constant, *S*-parameters.**

I. Introduction

THE continued growth of personal communications with wireless applications has generated a great demand for portable and highly integrated components and subsystems. As a consequence, these applications challenge semiconductor and packaging technologies to integrate high density 3-D mixed-signal integrated circuits on complex multilayer semiconductor substrates, assembled in multilayer packages and modules.

Frequently these substrates possess an inherently lossy characteristic, which deteriorates their performance or puts the accuracy of active and passive elements modeling under question. At frequencies where the dimensions are not electrically small, it is necessary to use complex distributed models. General full wave numerical methods such as FDTD, FEM, MoM and PEEC have been applied to model these structures successfully. The basic key to build successful models and perform genuine electromagnetic simulations of topology layout is the knowledge of complex characteristic impedance and propagation constant in transmission line structures on the upper interconnect levels. Ultimately, it is necessary for the IC industry to characterize these losses and novel dielectric properties of such sequenced isolation and semiconductor layers, with different thickness and relative dielectric permittivity, in order to build a representative interconnect characterization database [1]. The most reliable information about wave propagation in multilayer metal/dielectric/semiconductor systems is knowledge of the effective dielectric constant, derived straightforwardly from the propagation constant, more precisely its imaginary part – the phase constant.

Previous research has demonstrated *S*-parameter characterization of interconnect transmission lines, based on two-port unbalanced measurements, R_i-L_i-G_i-C_i modeling and extraction of characteristic impedance Z_C and propagation constant γ [1], [2]. The core of our approach is the same but differs in some aspects from the well-known procedure: a) we rather implement and measure one-port open-end stubs instead of relatively long transmission lines with two ports); b) short-end stubs are not included in the measurement test set-up in order to eliminate the inserted parasitic inductance of grounding through-hole vias and existing obstacle to build them by some technologies; c) two-port measurements are conducted on a transmission line with the same length, width and contact pads (launchers) geometry as the open-end stub; d) Z_C and γ are extracted directly from *S*-parameter data of the one-port capacitive (open) and inductive (short) stubs. In many cases, existing de-embedding structures and some of the TRL calibration standards in the test set-up could be easily implemented to acquire the necessary one-port stub *S*-parameters for calculations of the propagation constant. The effective dielectric constant is derived from the phase constant.

II. Theory of Transmission Line Stubs

Open and short stubs are widely used in microwave transmission line designs as capacitors, inductors or resonator tanks to ground. For example many DC biasing circuits implement stubs to achieve higher isolation between power supply and the RF signal. The size of the stubs is small enough to build LC filters and matching networks, when their length is smaller or equal to $n.(\lambda_{line}/4)$.

Conventional small signal *z*-, *y*-, and *ABCD*-parameters, are not quite suitable for high frequency interconnect characterization, because "open" and "short" terminations, required to measure this data, cannot be easily implemented in "on-wafer" applications and deteriorate performance by

Radosvet G. Arnaudov is Head of MMIC Department with the company "RaySat BG" and Associate Professor in TU-Sofia at the dept. of Microelectronics, both in Sofia, Bulgaria (phone: +359 2 9625665, e-mail: RadosvetA@gilat.com).

Radoslav B. Borisov is MMIC Designer at "RaySat BG" and currently making his Ph.D. in the field of Microeletronics (e-mail: RadoslavB@gilat.com).

insertion of impedance parasitics. The "short" circuit terminations possess excessive parasitic inductance of GND vias, while "open" ones have external capacitance, due to the fringing effect of the edge electric field at higher frequencies. *S*-parameter measurements, defined in terms of incident and reflected waves in a controlled 50-Ω measurement system, reliably characterize interconnect high frequency responses.

The input impedance Z_{in} of a given interconnect transmission line can be readily derived from the simulated or measured two-port *S*-parameters [2]. Placing the *S*-parameters in a schematic simulator and providing ideal ground connection at one of the ports can give us information about the input impedance, when the line is shorted to ground. The same is valid if one of the ports is left open.

$$\dot{Z}_{input\ short\ stub} = Z_0 \cdot \frac{1 + S_{11\,short}}{1 - S_{11\,short}} \quad (1a)$$

$$\dot{Z}_{input\ open\ stub} = Z_0 \cdot \frac{1 + S_{11\,open}}{1 - S_{11\,open}} \quad (1b)$$

From transmission line theory and Telegrapher equations $Z_{input\ short}$ and $Z_{input\ open}$ for short lines with length $l < \lambda/4$ the input impedance is defined from the equivalent circuit in Fig. 1.

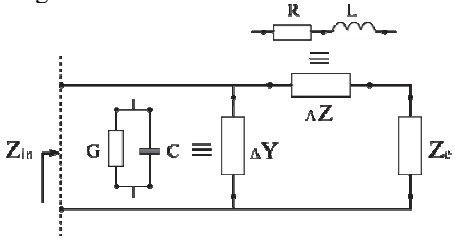

Fig. 1. Equivalent circuits of Telegrapher equations: simple Γ-type representation of transmission line (TRL) with length Δl→0.

On the other hand, expression of the input impedance of one regular two-conductor and lossy transmission line, when the load Z_L is 0 (short) or ∞ (open), could be presented as:

$$\dot{Z}_{input\ short} = \dot{Z}_C \tanh(\gamma \cdot l) \quad (2a)$$

$$\dot{Z}_{input\ open} = \dot{Z}_C / \tanh(\gamma \cdot l) \quad (2b)$$

The first equation defines the losses in the TRL metal layers and includes skin-effect. The second equation is connected to the substrate dielectric losses, caused by leakage in the substrate (tanδ) or some semiconductor conductivity σ.

Let us equalize input impedances from (1a) and (2a). The same is valid for (1b) and (2b). For simplicity we shall work from now further on with:

$$\dot{Z}_{input\ short\ stub} = \dot{Z}_{input\ short}\ ;\ \dot{Z}_{input\ open\ stub} = \dot{Z}_{input\ open} \quad (3)$$

After multiplying (2a) and (2b) and substituting $Z_{input\ short}$ and $Z_{input\ open}$ from equation (1a) and (1b), we obtain the following expressions for the characteristic impedance Z_C, where Z_0 is the system impedance 50 Ω:

$$\dot{Z}_C = \sqrt{\dot{Z}_{input\ open} \cdot \dot{Z}_{input\ short}} \quad (4a)$$

$$\dot{Z}_C = Z_0 \cdot \sqrt{\frac{(1 + S_{11short}) \cdot (1 + S_{11open})}{(1 - S_{11short}) \cdot (1 - S_{11open})}} \quad (4b)$$

After some algebra transformations by substitution of (1), (2) and (3) in (4) is obtained:

$$X = \sqrt{\frac{\dot{Z}_{input\ short}}{\dot{Z}_{input\ open}}} = \frac{\dot{Z}_{input\ short}}{\dot{Z}_C} = \frac{\dot{Z}_C}{\dot{Z}_{input\ open}}, \quad (4c)$$

where X is a hyperbolic tangent of the propagation constant γ multiplied by the physical line length l:

$$\tanh(\gamma . l) = \sqrt{\frac{\dot{Z}_{input\ short}}{\dot{Z}_{input\ open}}} \quad (4d)$$

Effective dielectric constant is a function of the shape and electro-physical transmission line parameters and β can be extracted from the imaginary part (phase constant) of the complete propagation constant γ.

From $\beta = 2\pi / \lambda_{line}$ where $\lambda_{line} = \lambda_0 / \sqrt{\varepsilon_{eff}} = c_0 / f \cdot \sqrt{\varepsilon_{eff}}$ we manage the following expression for ε_{eff}:

$$\varepsilon_{eff} = \left[\frac{imag(\gamma) . c_0}{\omega} \right]^2, \quad (5)$$

where ω – angular frequency, γ – propagation constant and c_0 is light velocity in free space.

Imaginary part of the propagation constant is the phase constant β. From (4d) the propagation constant is:

$$\gamma = \frac{1}{l} a \tanh \sqrt{\frac{\dot{Z}_{input\ short}}{\dot{Z}_{input\ open}}}, \quad (6)$$

where l is physical length of the transmission line, $Z_{input\ short}$ is the input impedance obtained from (1a) and $Z_{input\ open}$ is the input impedance obtained from (1b).

After substitution of (6) into (5) ε_{eff} is directly derived.

III. Experimental Results and Measurements

A. EM Simulations of Semi-insulating Substrate GaAs

Verification of the proposed method was done through electromagnetic simulations and measured *S*-parameters of microstrip transmission lines on GaAs and SiGe structures. In the presented work, investigation and comparison of the effective dielectric constant ε_{eff} and characteristic impedances Z_C are achieved by method of moments (MoM) implementation in EM simulations and "on-wafer" probe station measurements.

Simulation parameters of the semiconductor substrates are given in Fig. 2. The main difference is the conductivity of both substrates. In this work for the conductivity of the GaAs substrate is taken σ = 0.2 S/m. Typical conductivity of SiGe substrates varies between 10 - 30 S/m and in our case σ = 25 S/m.

Fig. 3 and Fig. 4 present the simulations of microstrip lines on non-conductive (semi-insulating) substrate in the frequency range 1 – 40 GHz and line widths: 5 μm, 10 μm, 15 μm, 30 μm, 60 μm. For each width additional simulations were performed with varying lengths of 30 μm, 100 μm, 150 μm, 200 μm and 300 μm.

Simulated results for semi-insulating GaAs prove that the length of the transmission line doesn't have a significant effect over ε_{eff} and Z_C. Effective dielectric constant varies from 6.5 to 4.7 with the change of width. This means that with the increasing width of transmission lines the capacitive coupling between the top metal layer and bottom ground increases, too. From electromagnetic

point of view - more energy from the electromagnetic TEM-wave will be enclosed within the substrate between active conductor and reference ground plane.

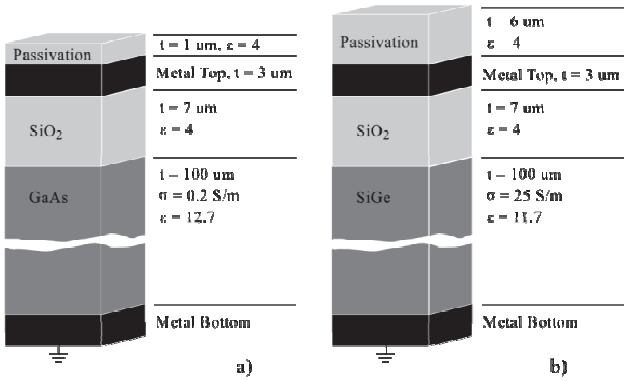

Fig. 2. Multilayer dielectric/semiconductor substrates applied in electromagnetic simulator for extraction of S-parameters: a) semi-insulating substrate – GaAs. b) conductive substrate - SiGe.

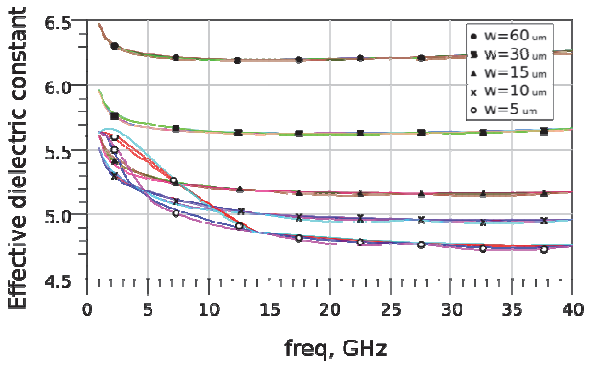

Fig. 3. Effective dielectric constant ε_{eff} of MSL on non-conductive substrate (GaAs); width W_x = 5, 10, 15, 30, 60 µm; length L_x = 30, 100, 150, 300 µm @ each W_x. EM simulations of structure on Fig. 2.a).

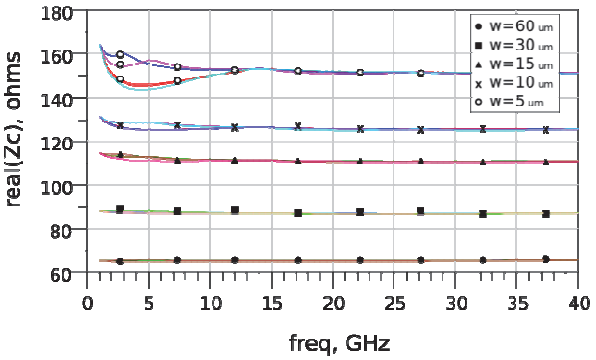

Fig. 4. Real part of Z_C for MSL on non-conductive substrate (GaAs); width W_x = 5, 10, 15, 30, 60 µm; length L_x = 30, 100, 150, 300 µm @ each W_x. EM simulations of structure on Fig. 2.a).

The same simulations have been performed for conductive substrate as SiGe shown in Fig. 2.b). Results are depicted in Fig. 5 and Fig. 6.

B. EM Simulations of Conductive Substrate SiGe

The exact analysis of microstrip line build on conductive substrates is given in [3], where the existence of three fundamental modes i.e. "dielectric quasi-TEM mode", "skin-effect mode" and "slow-wave mode" is demonstrated, and the conditions for appearance of each mode are clarified by the bulk resistivity of substrate/frequency dependence. When the product of frequency and resistivity of the Si-substrate is large enough to produce a small dielectric loss angle, the substrate acts like an isolating dielectric and TEM mode occurs. When the product of the frequency and the substrate resistivity is low enough to yield a small depth of EM-field penetration into silicon, the semiconductor substrate would behave like a lossy conductor wall, and the line may be treated as a MIM (metal-insulator-metal) microstrip line onto an imperfect "ground plane". Hence EM-fields don't penetrate deeply in the silicon and only a thin "skin" layer carries the main current – "skin-effect mode" propagation takes place. At frequencies which are not so high and the resistivity is moderate, the substrate acts like none of the above cases and "slow-surface wave" propagates along the line. This leads to a huge increase of the effective dielectric constant, even several tens or hundreds.

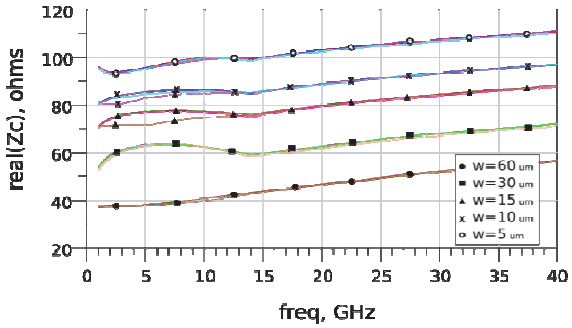

Fig. 5. Real part of Z_C for MSL on conductive substrate (SiGe); width W_x = 5, 10, 15, 30, 60 µm; length L_x = 30, 100, 150, 300 µm @ each W_x. EM simulations of structure on Fig. 2.b).

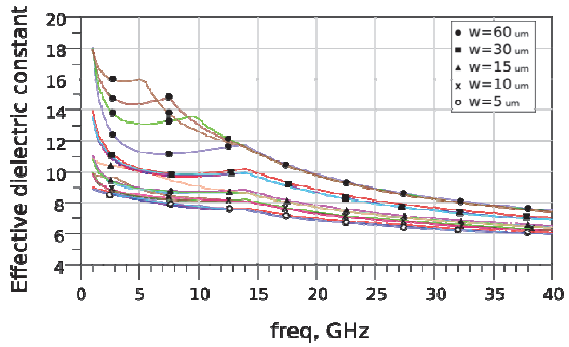

Fig. 6. Effective dielectric constant ε_{eff} of MSL on conductive substrate (SiGe); width = 5, 10, 15, 30, 60 µm; length L_x = 30, 100, 150, 300 µm @ each W_x. EM simulations of structure on Fig. 2.b).

For lower frequencies and wider transmission lines, the effective dielectric constant looks like ε_{eff} of a capacitor with a slightly conductive dielectric between the plates. In such a case this is reasonable for "skin-effect mode" and the transmission line acts like a microstrip line without "ground plane". For higher frequencies the product of dielectric loss-angle and substrate is large enough and the substrate acts like isolating dielectric. In that case ε_{eff} varies between 6-18 and the real part of Z_C from 40 –110 Ω. For both substrates the imaginary part of Z_C is small and the simulated impedances alter from -30 to 10 Ω in the frequency range.

C. *Verification Measurements and Test Set-up*

Verification measurements using a network analyzer and GaAs test structures were conducted. In Fig. 7 is given the lay-out of such test structures, analyzed by the proposed methodology. *S*-parameters measurements of sample transmission line by means of VNA "HP 8510C" network analyzer and probe station "Cascade Microtech RF1" were carried out. The VNA calibration software makes the analysis of the structure and extracts the effective dielectric constant for the calibrated bandwidth in a single S1P file. Using this file and the extracted parameters of transmission-reflect-line (TRL) calibration data, a comparison between the VNA results and described methodology was carried out. The graphics are pointed out in Fig. 8.

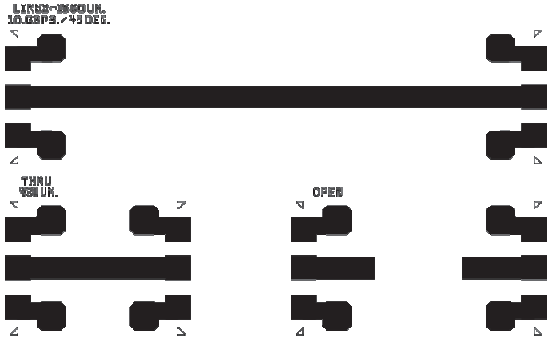

Fig. 7. Photo mask of microstrip lines on GaAs wafer, applied in thru and reflect (open) standards for TRL calibration in 10-30 GHz band.

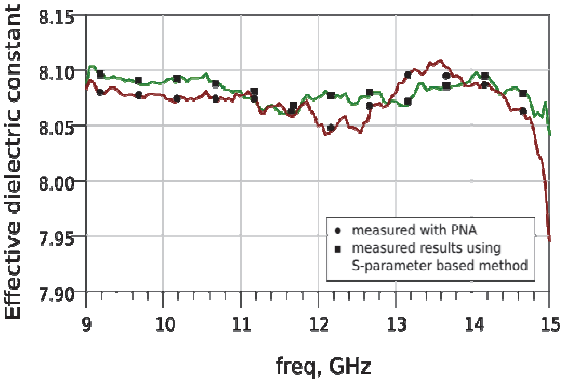

Fig. 8. Comparison of on-wafer measured (circle dots) and by this method extracted ε_{eff} of microstrip transmission line on GaAs substrate from Fig. 7.

Algorithm for extraction of microstrip TRL ε_{eff}:

1. Measure the scattering parameters S_{11}, S_{21}, S_{12} and S_{22} of microstrip TRL (W_x, $L_x < \lambda_{line}/4$);
2. Place in circuit simulator and find $S_{ii\ open}$ and $S_{ii\ short}$;
3. Use (1a) and (1b) to find $Z_{input\ short\ stub}$ and $Z_{input\ open\ stub}$;
4. Use (4) to find Z_C of the transmission line (TRL);
5. Measure the geometry length of the TRL and find the propagation constant γ by means of (6);
6. Substitute γ in (5) and extract the effective dielectric constant ε_{eff}.

The algorithm of the proposed extraction could be modified in the following way. Item 1 can be substituted with:

- One-port measurements of the "open" stub by means of the set-up in Fig. 9.a) or Fig. 9.c).
- There is an option to include one-port measurement of "short" stub by means of the set-up in Fig. 9.d). Thus the "artificial" obtaining of "short" stub by a circuit simulator from two-port measured *S*-parameters data of the transmission line (W_x, L_x) is omitted.

Using this algorithm and calibration structures it is possible to extract ε_{eff} for transmission line configurations with lengths L_x and widths W_x. In Fig. 9.a) is shown a microstrip TRL stub. One-port measurement can give us information about the input impedances when the TRL is open. Two-port measurements using TRL standards "thru" and "open", like those depicted in Fig.9.b) and Fig. 9.c), provide us enough information for extraction [5].

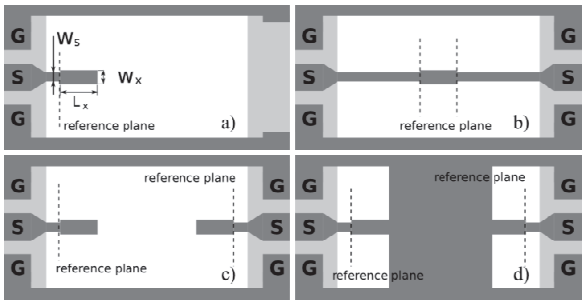

Fig. 9. Pictures of existing "on-wafer" test structures for extraction of ε_{eff}. a) One-port measurement of the investigated "open" stub; b) Two- port measurement of the investigated stub as a transmission line; c) De-embedding structure with two "open" stubs; d) De-embedding structure with two "short" stubs. Reference planes are determined by calibration.

The pictures of Fig. 9 are generated from mask design and dark-grey colour designates the top-level metal, while the light-grey colour shows the intermediate layer of shield metal on the interface dielectric-semiconductor. Blank white spaces under the actual microstrip lines are substrate back-side GND metal. Shifting of the reference planes is obtained after calibration and de-embedding of the ground-signal-ground (G-S-G) launchers.

In the following Fig. 10 a), b) and c) are depicted cross-sections of HFSS models for 3-D full-wave EM simulations of microstrip lines, built on Si-substrate. Basic features are: substrate conductivity σ = 25 S/m, microstrip width w = 20 μm, substrate height $h = d_{Si}$ = 400 μm and ε_r = 11.7, SiO_2-layer thickness d_{SiO2} = 6-7 μm and ε_r = 4.

When taking a closer look at the pictures of *E*-field intensity distribution, it is observed that the electrical field penetration into the depth of bulk silicon body (under the metal line), tends to increase in magnitude with frequency rising. At 1 GHz the intensity is very weak, while at 10 and 20 GHz the magnitude increases about 2 and 10 times respectively (in one and the same volume), assuming 1-D depth of penetration along the *z*-axis (boundaries 0 and h). Proper TEM-wave properties are demonstrated at 10 and 20 GHz, while below 1-7 GHz region and microstrip widths of 20-60 μm there exists one transition zone of slow-wave propagation (see Fig. 12), where ε_{eff} is greater than ε_r of the bulk material (SiO_2/Si) combination – equations (9), (10).

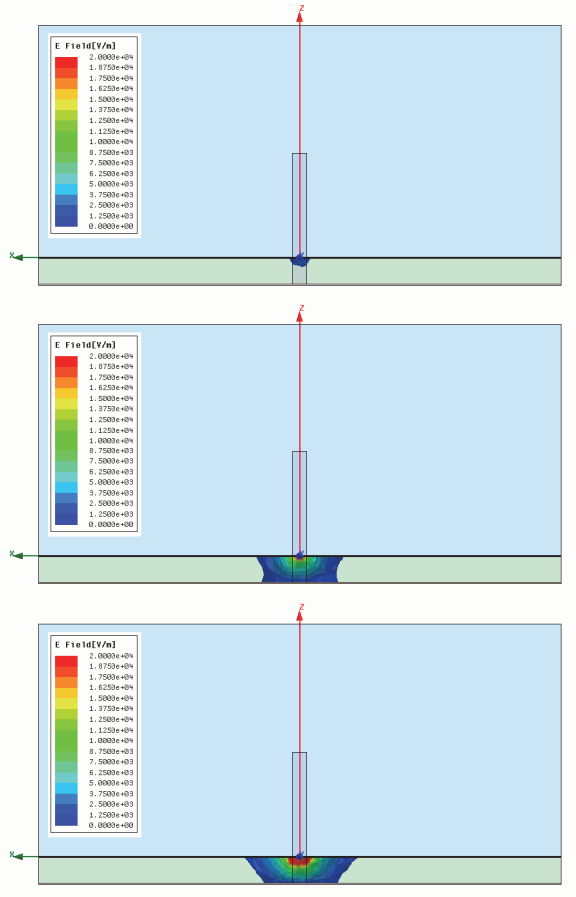

Fig. 10. Intensity distribution of E-field, excitation by 2-D wave port on the *x*-*z* plane with dimensions $W' = (3\text{-}5).w$ and $H' = (5\text{-}10).h$ a) *E*- vector at 1 GHz; b) *E*-vector at 10 GHz; c) *E*-vector at 20 GHz.

If we approximate a linear type of charge density distribution $\rho = \rho_0.z$ (ρ_0 is a constant of function slope) under the SiO_2/Si-interface, 1-D gradient potential function approach along the *z*-axis and maximum *E*-field magnitude $E_{max}=-V_{max}/h$ at the boundary metal-dielectric, we can derive the following expression, leaning on the Poisson equation. The substitution $E= -\text{grad}(\Phi)$ is applied:

$$\frac{\partial^2 \Phi}{\partial^2 z} = -\frac{\rho}{\varepsilon} \tag{7}$$

Double integration of the above expression is performed and after the determination of the integration constants we obtain a general equation for *E*, from which (8) follows:

$$\varepsilon = \frac{\rho_0 (3z^2 - h^2)}{6(E + \frac{V}{h})} \tag{8a}$$

$$E_{\max} = \frac{\rho_0 h^2}{3\varepsilon} - \frac{V}{h} \tag{8b}$$

$$V = -\frac{\rho_0 h^3}{6\varepsilon} \tag{8c}$$

The values of the potential function Φ are *V* and 0 at the boundaries top metal strip-dielectric (z=h) and dielectric-ground metal (z=0), respectively. Equations (8b) and (8c) are derived for these boundary conditions. It is easily seen that the absolute dielectric permittivity $\varepsilon=\varepsilon_0.\varepsilon_r$ of the media is inversely proportional to the applied electric field. In our case as *E* decreases, ε increases (in one and the same constant volume) and at certain conditions this value could exceed ε_r, "slow" and "skin" wave effects occur.

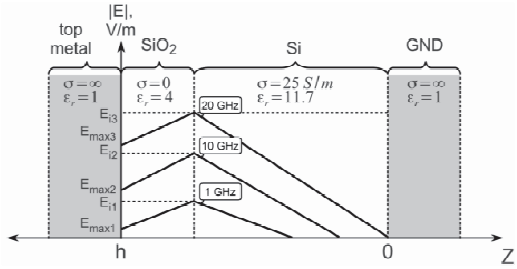

Fig. 11. Illustration of the E-field distribution along the *z*-axis of the HFSS model cross-sections in Fig. 10.a), Fig. 10.b) and Fig. 10.c). Polarization charge accumulation on the interface Si/SiO_2 is due to the Maxwell-Wagner effect. Graphs are not in scale.

D. Discussion on Conductive Substrate Peculiarities

It is a well-known fact from transmission line theory and Telegrapher equations that each parallel-plate inter-connection line can be described fully by its complex characteristic impedance Z_C and propagation constant γ through its equivalent p.u.l. (per-unit-length) distributed R_i-L_i-G_i-C_i elements. Equations (1)-(6) are consistent with TEM-wave propagation in such a structure, because they are based on the Telegrapher equations solution for long two-conductor transmission lines with a regular shape. Thus microstrip and embedded microstrip line structures fall into consideration by the presented work. So the obtained results for ε_{eff} in (5) may be determined also as dependent on the width W_x (perpendicular to wave direction), substrate thickness *h* and relative dielectric constant ε_r [4]. The effect of fringing electric field is taken into consideration.

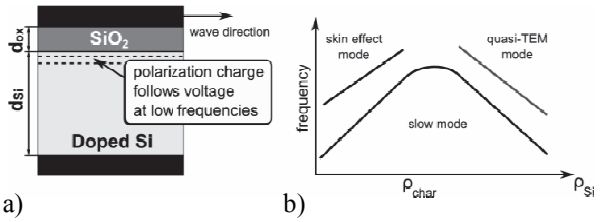

Fig. 12. a) Illustration of polarization charge accumulation on the interface Si/SiO_2; b) EM-wave propagation mechanism as a function of frequency and substrate bulk resistivity.

However, the Si/SiO_2-sandwich does not obey the property to support propagation of TEM-waves only. Actually from a macroscopic point of view, the Si-substrate acts like a conductor for voltage changes between the metal layers, and these changes are followed by charge accumulation at the Si/SiO_2-interface, up to frequencies of few GHz (depending on the doping level of silicon). Hence, the distributed C_i is equal to the oxide capacitance per unit length, depends mostly on d_{ox} and very slightly on d_{Si}. In contrast, the inductance L_i depends on the distance between metal planes of the microstrip structure, hence on $d_{ox}+d_{Si}$. Due to these different dependencies L_i remains roughly the same as for the TEM-mode, but C_i is much higher, especially if $d_{ox}<<d_{Si}$. Thus the effective dielectric constant can be as high as hundreds or more, much higher than the relative dielectric

permittivity of Si (11.7) and SiO_2 (4). This effect is described by the so-called Maxwell-Wagner polarization mechanism, which results in much higher values of the effective dielectric constant for "slow-wave" propagation [3].

$$\varepsilon'_{effSW} = \varepsilon_0 \frac{\sum_{i=1}^{n} d_i}{d_i} \varepsilon_{ri} = \varepsilon_0 \varepsilon_{s0} \tag{9}$$

$$\varepsilon'_{effTEM} = \varepsilon_0 \left(\sum_{i=1}^{n} d_i\right) \left(\sum_{i=1}^{n} \frac{d_i}{\varepsilon_{ri}}\right)^{-1} = \varepsilon_0 \varepsilon_{s\infty} \tag{10}$$

$$\rho_{char} = \sqrt{\frac{\mu_0 d_{ox} d_{Si}}{3\varepsilon_0 \varepsilon_{SiO_2}}} \tag{11}$$

In equations (9) and (10) are given expressions for the absolute values of the effective dielectric constants, indexed *SW* – for "slow" and "skin-wave" propagation and *TEM* for TEM-wave, respectively. Here d_i is the thickness of each layer, ε_{ri} relative constant of corresponding layer material. It can be proved that values from (9) can be much greater than the relative ones ε_{ri}, while on the contrary in (10) ε_{ri} is their upper limit. Equation (11) exhibits the so-called "characteristic" bulk resistivity of semiconductor, at which the maximum "slow-wave" frequency is reached (see Fig. 12. b)). In the literature ε_{s0} is called static Maxwell-Wagner permittivity and $\varepsilon_{s\infty}$ – optical value of it. The latter is easily developed from applying a series connection of capacitors with identical areas, different thicknesses and extracting their equivalent capacitance ε_{req}. In summary, when TEM-wave propagates a displacement current in the structure prevails, while in the other modes conduction currents in metal and semiconductor skin-layers are predominant.

An important comment may be included here, a polarization effect takes place when the substrate does not possess properties of perfect insulator dielectric, on the contrary, there exists a certain amount of free carriers (holes or electrons), depending on the semiconductor doping level and type. From a microscopic point of view, some more explanation can be added to the above statements. Due to the field-effect of MOS/MIS/MESFET gate structures, when biased with DC potential + RF signal, regions with accumulated minor carriers (enhancement mode and inverse channel) or depleted major carriers (depletion mode) are formed [6]. The thickness of such a boundary region on dielectric-semiconductor interface varies according to the DC voltage value and polarity, magnitude of RF voltage swing, substrate doping level and channel modulation may occur. This could be the source for building of distributed microwave active devices as detectors, voltage-controlled filters and attenuators, etc.

IV. Conclusions

A methodology for simple extraction of effective dielectric constant in microstrip transmission lines on multilayer substrates, from measured or simulated S-parameters data, using on-chip test structures, has been demonstrated. The basic key to build successful models and perform genuine electromagnetic simulations of IC topology layout is the knowledge of complex characteristic impedance and propagation constant. The effective dielectric constant is derived from the phase constant. This method is capable to be implemented in LTCC and LCP substrate material evaluation for IC packaging purposes, also.

Fundamentals of the presented method can be referred to the so-called "direct" ones as far as *S*-parameter measurements or simulations of the investigated structures are concerned. The chosen approach of "open" and "short" transmission line stubs, with length less than one quarter wavelength, is mandatory in order to mitigate resonance phenomena, where indefiniteness of the input line impedance exists and particularly tan(βl) is 0 or ∞. In such cases is recommended the implementation of "indirect" methods, which are based on inserting of sample material in bulk waveguide resonators or building transmission line resonators on the investigated material.

As far as "open" stubs are dealt with, a reasonable question about inserted equivalent electrical "elongation", due to the fringing electrical field at the edges, may arise. The conducted experiments show that such phenomena in thin semiconductor substrates (100-400 μm) and relative dielectric constants in the range of (9-13), cannot cause considerable errors in the achieved data. Nevertheless, in order to eliminate such possibilities, we have the opportunity to omit one-port open-stub measurements and rely on the two-port measured *S*-parameters data of TRL (see Fig. 9.b)) with subsequent "artificial" conversion to "open" and "short" stub data in the circuit schematic simulator. This mathematical operation is absolutely free of errors, because of the implementation of ideal "open" (perfect magnetic wall) and "short" (perfect electrical wall).

A practical conclusion can be summarized from Fig. 11. When a true TEM-wave propagates in the structure, the value of *E*-vector magnitude is 0 exactly at the interface boundary of dielectric-GND metal plate, while if some other mixed modes exist there is a shift upwards into the dielectric body and physical substrate thickness *h* converts into h_{eff}, i.e. the graphs for 1 and 10 GHz. This effect is observed for dielectric substrates with some conductive features, where h_{eff} differs from *h*.

References

[1] W. R. Eisenstadt and Y. Eo, "S-Parameter-Based IC Interconnect Transmission Line Characterization," *IEEE Trans. Comp. Hybrid, Manuf. Technol.,* vol. 15, no. 4, pp. 483-490, Aug. 1992.

[2] Yungseon Eo and W. R. Eisenstadt, "High-Speed VLSI Interconnect Modeling Based on S-Parameter Measuraments," *IEEE Trans. Comp. Hybrid, Manuf. Technol.,* vol. 16, no. 5, pp. 555-562, Aug. 1993.

[3] Hideki Hasegawa, M. Furukawa, and H. Yanai, "Properties of Microstrip Line on Si-SiO_2 System," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-19, no. 11, pp. 869-881, Nov. 1971.

[4] R. Garg, P. Bhartia, I. Bahl, and A. Ittipiboon, *Microstrip Antenna Design Handbook*, Norwood, U.S.A.: Artech House Inc., 2001.

[5] Ming-Hsiang Cho, Guo-Wei Huang, Chia-Sung Chiu, Kung-Ming Chen, An-Sam Peng, and Yu-Min Teng, "A Cascade Open-Short-Thru (COST) Method for Microwave On-Wafer Characterization and Automatic Measurements," *IEICE Trans. Electron.*, vol. E88-C, no. 5, pp. 845-850, May 2005.

[6] M. Gospodinova, V. Mollov, and R. *et al* Arnaudov, "Study of the DC Biasing Effect on Insertion Losses in High-frequency Interconnections", *Elsevier Microelectronics Journal, Netherlands,* vol. 31/11-12, Nov. 2000, pp. 1009-1014, ISSN 0026-2714.