

Reduced-Complexity Offset Min-Sum Check Node Unit for Layered 5G LDPC Decoder

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Abstract — This paper presents a novel approach for the reduced-complexity Min-Sum (MS) decoding of low density parity check (LDPC) codes in the partially parallel layered decoder architecture, which contains a large number of serial check node processors. Reduced complexity is obtained by using the variant of the single-minimum Offset Min-Sum (smOMS) algorithm that approximates a second minimum with the addition of the variable weight parameter to the minimum value. Although the reduced-complexity MS algorithms primarily reduce hardware resources in fully parallel implementations, the results showed that a considerable reduction can be obtained if serial check node processors are used. The paper also proposes a better subminimum estimation for irregular codes from 5G new radio (5G NR). The method uses smaller subminimum estimation weights in check nodes with a higher degree and higher weights in check nodes with a smaller degree, which leads to the significant improvement in the SNR performance. Additionally, it is shown that SNR performance can be further improved by applying offset before minimum calculation, which differs from conventional Min-Sum approaches.

Keywords — 5G new radio, layered decoding, low density parity check (LDPC) codes, min-sum (MS) algorithm.

I. INTRODUCTION

FIFTH generation (5G) New Radio (NR) uses low density parity check (LDPC) codes [1] for channel coding on the data channel [2]. These codes belong to the family of quasi cyclic (QC) LDPC codes whose parity check matrix (PCM) is consisted of circularly shifted identity sub-matrices [3]. Such structure is convenient for achieving high parallelism in the decoder implementations, which is the key prerequisite for obtaining a high throughput required by modern communications. 5G NR codes are constructed based on the base graph matrix, which determines positions of the circularly shifted identity submatrices [4]. Additionally, the code is defined by the

size of the identity sub-matrix (lifting size), and by shift values for each submatrix in the code's PCM.

LDPC codes are usually decoded using the message passing algorithm [5], which provides a good capacity approaching performance [6]. Multiple approximations to the original message passing algorithm are frequently applied in implementations of LDPC decoders in order to reduce the complexity of calculation. Some of the most frequent approaches are the min-sum (MS) algorithm [7] and, its variants, Offset MS (OMS) and Normalized MS (NMS) [8]. In the message passing algorithm, nodes in the LDPC codes' Tanner graph communicate using messages that are iteratively exchanged between variable and check nodes until the decoding is finished or until the maximum number of iterations is reached. In the MS algorithms check nodes calculate two minimum magnitude variable-to-check messages and return check-to-variable messages based on these two values.

Although MS algorithms give high complexity reduction compared with the original message passing algorithm, a further reduction can be made if only one minimum is calculated and if the second one is only approximated [9]–[13]. This can lead to significant hardware resource savings, especially when check node processes all messages in parallel [10]–[13]. A single minimum MS (smMS) is presented in [9], where the second minimum is estimated by an addition of a constant weight parameter to the minimum value. This is the simplest approach, but suffers from high error floors. A variable weight smMS (vwsmMS) is presented in [10], where the weight parameter is increased during the decoding, since the actual difference between the subminimum and the minimum in the MS algorithm increases in each new iteration of the decoding. Such an approach gives a significantly better signal-to-noise ratio (SNR) performance. If all messages are simultaneously available at the check node, even better results can be achieved by approximate finding of the subminimum value in the minimum finder tree [10]–[13].

Although fully parallel architectures give the highest throughput, the hardware complexity due to routing congestion can be high [14]. This paper presents a study on the reduced-complexity decoding for 5G NR in the partially parallel architectures. Such architectures have check node units (CNUs) that do not receive all messages in parallel, but serially [15], [16]. However, due to the high lifting size of the matrix, there are many of these serial CNUs. The chosen architecture performs a layered decoding schedule which updates the variable nodes more frequently than the original message passing algorithm and provides faster convergence [17].

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This paper presents a reduced-complexity OMS decoding, which is based on the vwsms, but is improved by a different choice of weights specific for irregular 5G NR LDPC codes. In addition, the architecture of the serial check node unit that implements the improved reduced-complexity algorithm is presented. These contributions have already been presented in [18]. In the present work, the check node processing is improved for a better SNR performance, whereas the hardware complexity is kept reduced. Moreover, the SNR performance analysis is expanded to three 5G NR LDPC codes for better understanding of possible applications of the proposed method.

The rest of the paper is organized as follows. Section II presents Offset Min-Sum algorithm for decoding of LDPC codes and previous approaches for complexity reduction of the OMS algorithm. The outline of the proposed method for reduced complexity OMS decoding of 5G LDPC codes is presented in section III. In section IV the proposed method is further analyzed and the hardware architecture for the implementation of the algorithm is presented. Results for both SNR performance and hardware complexity are presented in section V. Conclusion is given in section VI.

II. DECODING ALGORITHMS IN LAYERED LDPC DECODERS

A. Offset Min-Sum layered decoding

The iterative OMS decoding [8] consists of the initialization, check node updates and variable node updates. Firstly, the variable nodes v are initialized by the input a priori log-likelihood ratio (LLR) values calculated as

$$LLR_v = \log \frac{P(b_v = 0 | y_v)}{P(b_v = 1 | y_v)} = \frac{2y_v}{\sigma^2}, \quad (1)$$

where y_v are the channel outputs, σ^2 is the channel noise variance and $P(b_v = b | y_v)$ is the conditional probability that the bit b_v is equal to b , given that the y_v is received. After initialization variable nodes send messages to check nodes which in the first iteration are equal to the input LLRs ($M_{v2c} = LLR_v$). In layered schedule [17], messages are not exchanged simultaneously. The PCM is divided into layers and the first group of messages is sent to the check nodes from the first layer (eg. in QC-LDPC all check nodes that correspond to the first row in the base graph matrix). Check nodes calculate their response and send messages to variable nodes as

$$M_{c2v} = \max \left(\min_{v' \in V_c \setminus v} (|M_{v'2c}|) - \beta, 0 \right) \times \prod_{v' \in V_c \setminus v} \text{sgn}(M_{v'2c}), \quad (2)$$

where V_c is the set of all variable nodes connected to the check node c , and β is an offset parameter. Based on newly received check-to-variable messages and already sent variable-to-check message, variable nodes update LLR values as

$$LLR_v = M_{v2c} + M_{c2v}. \quad (3)$$

In the next sub iteration, a new layer is processed; variable

nodes send new messages calculated as

$$M_{v2c} = LLR_v - M_{c2v}. \quad (4)$$

Check-to-variable messages in (4) are zero in the first iteration, but in every other iteration they are check-to-variable messages from the previous iteration.

B. Reduced complexity offset Min-Sum

As can be seen from (2) the CNU should find two variable-to-check messages of least magnitude, select one of them, modify it with the offset parameter and pass it with the sign determined by the sign product as a new check-to-variable message. Reduced complexity can be achieved if only one minimum is calculated and the other estimated as

$$M_{c2v} = \max(M - \beta, 0) \times \prod_{v' \in V_c \setminus v} \text{sgn}(M_{v'2c}), \quad \text{where} \\ M = \begin{cases} \min_{v' \in V_c} (|M_{v'2c}|) + w, & \text{if } \min_{v' \in V_c} (|M_{v'2c}|) = |M_{v2c}| \\ & \text{and } N_{min} = 1 \\ \min_{v' \in V_c} (|M_{v'2c}|), & \text{otherwise} \end{cases}, \quad (5)$$

where w is the weight factor for subminimum estimation and N_{min} is the number of message magnitudes that are equal to the minimum message magnitude [9]. If w is fixed during the decoding, the complexity is mostly reduced, but a significantly better SNR performance is obtained if w is increased in each iteration or at least after every few iterations [10]. A method with a fixed w is called single minimum OMS (smOMS), whereas the method with a variable w is called variable weight smOMS (vwsmsOMS). It should be emphasized that only these methods can lead to the reduced complexity for serial CNU. All other methods ([11]–[13]) calculate the subminimum and reduce complexity only of the parallel minimum finder but they are not able to reduce complexity of the serial CNU.

III. IMPROVEMENT OF THE REDUCED-COMPLEXITY OMS DECODING FOR 5G NR

LDPC codes from 5G NR are highly irregular [4], which means that variable node degrees (d_v) and check node degrees (d_c) are highly different for different nodes. The general structure of the base graph matrix for 5G NR LDPC codes is shown in Fig. 1. As can be seen, check node degrees vary from $d_c = 3$ to $d_c = 19$. Therefore, it can be expected that subminimum and minimum differences in the OMS algorithm would be larger for smaller degree nodes, since the number of values that enter the minimum calculation is smaller. This implies that the weight parameter w in the vwsmsOMS algorithm should be changed differently for check nodes with different check node degree. In order to confirm this assumption, a fixed-point implementation of the OMS decoder for (16128, 8448) code from 5G NR was simulated for multiple code words in an additive white Gaussian noise channel (AWGN). The average difference between subminimum and minimum for check nodes with different degrees is shown in Fig. 2. It is clear that higher degree check nodes have smaller differences between the subminimum and minimum values than the lower degree check nodes.

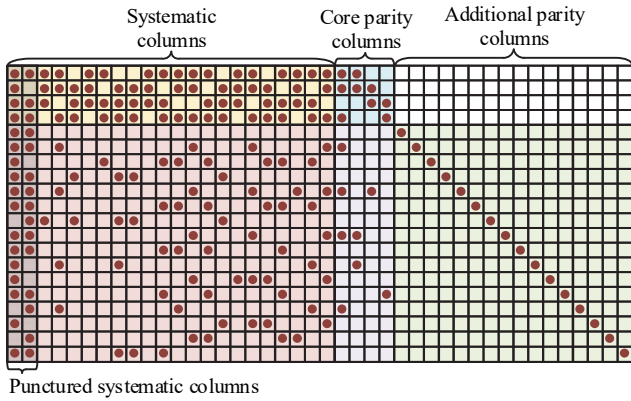


Fig. 1. The structure of the base graph 1 matrix of 5G NR LDPC codes. Dots represent the presence of the cyclically shifted identity matrix the PCM [18].

Interestingly, it is noticeable that high-degree check nodes' differences start decreasing near the end of the decoding. This is explained by the saturation of messages and LLRs in the fixed point implementation, because many messages have almost the same magnitude.

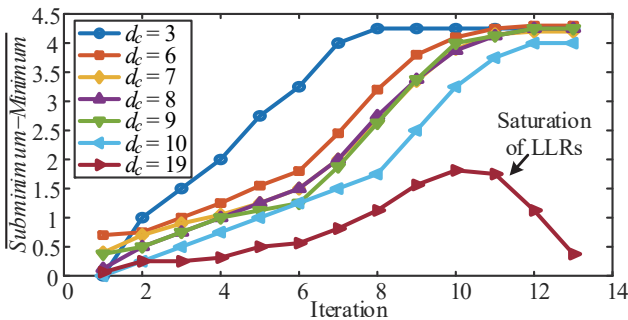


Fig. 2. The average difference of subminimum and minimum depending on the iteration number in fixed-point OMS layered decoding for 5G (16128, 8448) code [18].

Since the weight parameter w in the vwsmsOMS algorithm is already changing during the decoding, which is done in hardware by external setting of the parameter to all CNUs by the control, no additional complexity would be induced if w is changed separately for each layer too. Therefore, in this paper a vwsmsOMS is improved by setting the w parameter to a smaller value for higher degree check nodes. This is further called the enhanced vwsmsOMS (EvwsmsOMS).

As shown in (5), all single minimum OMS algorithms require information about the number of variable-to-check message magnitudes that are equal to the minimum message magnitude (N_{min}). In situations when this number is higher than 1, the subminimum is equal to the minimum message magnitude and the algorithm does not need to estimate the subminimum value, i.e. the subminimum value is calculated accurately. The more frequently this situation occurs, the more accurate is the algorithm, i.e. the more it behaves as the original OMS. In this paper a slight modification of (5) is proposed in order to achieve that aforementioned situations are more frequent. The check node unit processing is modified to

$$X_{v'} = \max(|M_{v'2c}| - \beta, 0), \quad X_{vmin} = \min_{v' \in \mathcal{V}_c} (X_{v'}),$$

$$|M_{c'2v}| = \begin{cases} X_{vmin} + w, & \text{if } vmin = v \text{ and } N_{min} = 1 \\ X_{vmin}, & \text{otherwise} \end{cases}, \quad (6)$$

$$M_{c2v} = |M_{c'2v}| \times \prod_{v' \in \mathcal{V}_c \setminus v} \text{sgn}(M_{v'2c}).$$

As shown in (6), the offset subtraction is moved to before the minimum calculation. The rest of the processing remains the same as in (5). Such modification provides that more values that enter minimum calculation are equal to 0. Therefore, the probability for equality of subminimum and minimum value is higher. The original OMS check node processing (2) would provide the same check-to-variable messages as in (6) if a subminimum and a minimum value are less than or equal to offset parameter β . Although these check-to-variable messages are 0 in such cases, the processing from (6) is therefore more accurate than processing from (5). In the rest of the paper, the algorithm from (6) will be called swapped (E)vwsmsMS and will frequently be marked with the suffix S.

IV. REDUCED-COMPLEXITY OMS CHECK NODE UNIT ARCHITECTURE

The conventional offset Min-Sum serial check node unit architecture is shown in Fig. 3. The CNU is consisted of two parts separated by pipeline registers. The input part calculates the minimum, subminimum, index of minimum, and sign product of all variable-to-check messages' signs. When minimums are found, the aforementioned values are written to pipeline registers, and input part starts doing calculations for the next layer. The output part selects one of the minimum or subminimum values, based on the minimum index value (if the check node sends the message to the variable node whose variable-to-check message was of minimum magnitude, then the subminimum is used). The selected value is then reduced by the offset parameter and saturated if the resulting value is less than zero. The sign of the check-to-variable message is determined based on the calculated sign product and the sign of the variable-to-check message from the variable node to which the check-to-variable message is sent, as in (2).

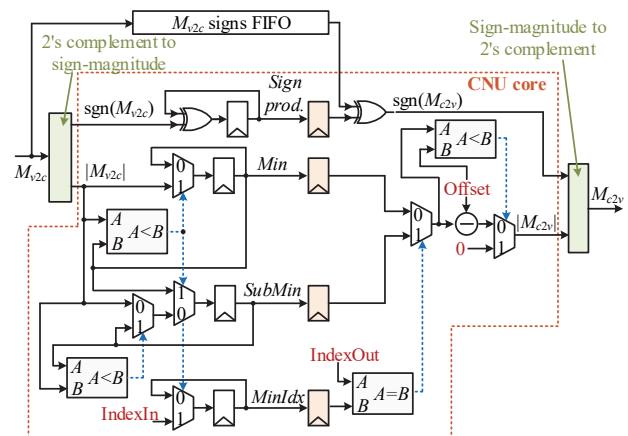


Fig. 3. Offset Min-Sum serial CNU architecture [18].

In the original reduced complexity EvwsmOMS implementation presented in [18], there is no need for calculation of the subminimum value. The proposed CNU architecture is shown in Fig. 4. The input part calculates the minimum, the index of the minimum and the sign product. Besides that, it needs to provide information whether the number of messages that have the same magnitude as the minimum is only 1 or more than 1, as required in (5). This is done using the equality output of the comparator. The *Eq.* signal is set to “1” whenever the current minimum and the new message magnitude are equal and reset whenever a new minimum is found. This way, the *Eq.* signal always tells if there is another variable-to-check message that is equal to the minimum. The comparator with the “less than” and “equal” outputs uses significantly less resources than two comparators necessary for both the minimum and subminimum calculation. Additionally, the number of flip flops is also reduced since the subminimum value is not kept.

Conventionally, the output part would calculate the estimated subminimum, and then use the minimum value and estimated subminimum in the same way as in the OMS architecture. This would require two addition operations and possibly, an unacceptable increase of hardware resources. The proposed architecture avoids this using the following procedure. The w parameter for subminimum estimation is already reduced by the offset parameter β , in order to avoid both the addition and the subtraction in cases when a subminimum should be passed. Instead of subtraction with the offset parameter, the output part performs a signed addition of the minimum and a negative offset ($-\beta$) or the already reduced weight parameter ($w-\beta$). If the resulting value is negative, the output should be saturated: to zero if the minimum is passed or to a maximum integer value if the subminimum is passed, because in the second case, the negative result means that the overflow has happened. If w is smaller than β , the negative values are saturated to zero.

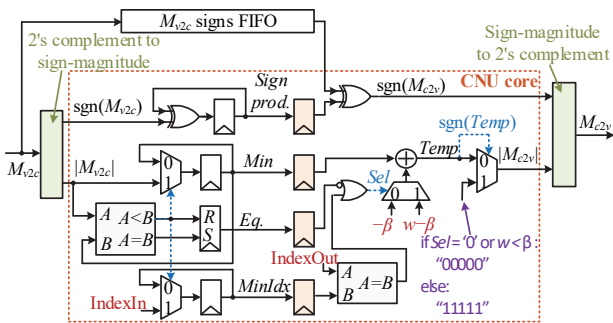


Fig. 4. EvwsmOMS serial CNU architecture [18].

The check node unit architecture for the modified swapped EvwsmOMS algorithm is shown in Fig. 5. As proposed in (6), the offset subtraction is done in the input part, immediately after the 2's complement to sign magnitude conversion. The rest of the input part is the same

as in Fig. 4. However, the output part of the CNU is now significantly simplified and has only the sign calculation and the selection of the minimum value or the subminimum estimation value.

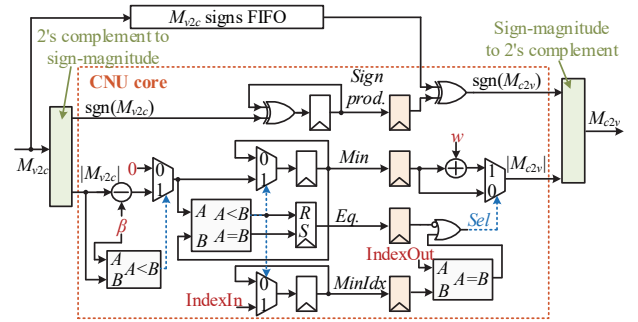


Fig. 5. EvwsmOMS serial CNU architecture with offset subtraction at the input.

V. RESULTS AND DISCUSSION

A. SNR performance

Monte Carlo simulations of the fixed point implementation of the multiple algorithms were performed for three codes from 5G NR: (21888, 8448), (14592, 8448), and (10752, 8448). Simulations were performed for AWGN channel and QPSK modulation, with 6 bits used for messages and 8 for LLRs. A maximum iteration number was set to 20. The simulated algorithms were MS, OMS, smOMS, vwsmOMS and enhanced vwsmOMS (EvwsmOMS) for both original and swapped versions. The MS algorithm is included in simulations since it also provides reduced complexity decoding with respect to the OMS. The complexity analysis is given in detail in subsection V.B.

In the reduced-complexity algorithms, weight parameters were changed as summarized in Table 1. In the smOMS, w was set to its best constant value, found by the systematic search. For vwsmOMS, w was changing linearly with the iteration number starting from $it = 0$. Linear functions from Table 1 gave the best results. Finally, the EvwsmOMS used various linear functions for nodes with different check node degrees.

Fig. 6 shows the simulated block error rate (BLER) curves. Firstly, it is apparent that the Min-Sum algorithm SNR loss is much higher at lower code rates than at higher code rates. In addition, when compared to the MS, all variable weight smOMS algorithms have a smaller loss with respect to the OMS at mid to low code rates.

When analyzing performance of EvwsmOMS, the results show a significant improvement with respect to the vwsmOMS, although the loss compared with the original OMS is still considerable. The loss is partially reduced if the swapped architecture is used. The offset subtraction repositioning provided the improvement between 0.1 dB and 0.2 dB, depending on the code.

TABLE 1: WEIGHT PARAMETERS USED IN SINGLE-MINIMUM OMS ALGORITHMS

Algorithm	5G NR Code					
	(21888, 8448)		(14592, 8448)		(10752, 8448)	
	d_c	w	d_c	w	d_c	w
smOMS	all	2	all	2.25	all	3.5
vwsmsOMS	all	$0.22 + 0.22it$	all	$0.22 + 0.22it$	all	$0.23 + 0.23it$
EvwsmOMS	3	$0.5 + 0.4it$	3	$0.5 + 0.4it$	3	$0.5 + 0.4it$
	4, 5	$0.25 + 0.25it$	6, 7, 8, 9, 10	$0.25 + 0.25it$	8	$0.25 + 0.25it$
	6, 7, 8, 9, 10	$0.25 + 0.22it$			19	$0.22 + 0.22it$
	19	$0.24it$	19	$0.23it$	19	$0.22 + 0.22it$

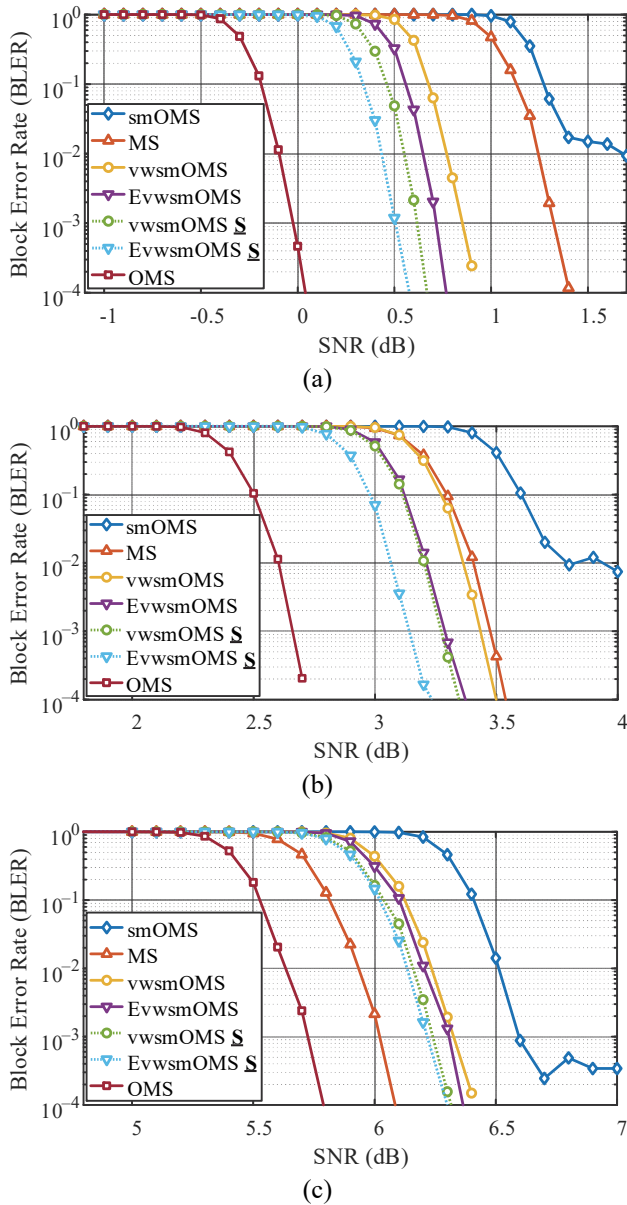


Fig. 6. SNR performance of various MS algorithms for base graph 1 codes from 5G NR: (a) Code rate 22/57 – (21888, 8448), (b) Code rate 22/38 (14592, 8448), and (c) Code rate 22/28 – (10752, 8448).

In the end, due to its very poor both error floor and waterfall region SNR performance, the smOMS with a constant weight factor is obviously inapplicable for 5G NR codes.

B. Hardware complexity

The proposed CNU core from section IV for the (E)vwsmsOMS algorithm and its swapped version, CNU core for OMS algorithm and CNU core for MS algorithm were implemented on the Zynq UltraScale+ RF-SoC device (XCZU28DR). The implementation results for 384 (maximum lifting size in 5G NR) CNU cores are shown in Table 2. Resource savings achieved in the (E)vwsmsOMS implementation compared with the OMS are about 35% for complex logic blocks (CLBs), 11% for look-up tables (LUTs), and 25% for flip flops (FFs). However, the swapped version of the (E)vwsmsOMS achieved resource savings of about 15% for complex logic blocks (CLBs), 19% for look-up tables (LUTs), and 25% for flip flops (FFs). Therefore, even though the serial CNU architecture is used, a considerable reduction in complexity can be achieved.

When compared to the MS implementation, single minimum approaches require more LUTs, but since they require a significantly smaller number of flip flops, the total number of used CLBs is still smaller.

TABLE 2: COMPARISON OF FPGA RESOURCES OF 384 CHECK NODE UNIT CORES FOR VARIOUS MS ALGORITHMS

Algorithm	CLBs	LUTs	FFs
MS	1547	5379	12288
OMS	1595	6934	12288
(E)vwsmsOMS	1032	6146	9216
(E)vwsmsOMS _{Swapped}	1357	5647	9216

VI. CONCLUSION

This paper has shown that reduced-complexity OMS decoding can be achieved in a partially-parallel LDPC decoder architecture with a considerable SNR performance loss. The proposed check node unit architecture provides significant resources savings compared with the conventional OMS approach. The paper also presents a better method for choosing the weight parameter used for estimation of the second minimum in the reduced-complexity OMS decoding. The weight parameter is chosen separately for check nodes with different check node weights since 5G NR codes are highly irregular. Using this method the SNR performance loss is partially reduced. In addition to that, the SNR performance loss is further improved by using a CNU architecture that repositions the offset subtraction to the input part of the CNU – before the minimum calculation.

Further work on this topic would include research on the optimal set of weight parameters used in variable weight single minimum OMS algorithms, which would provide further reduction of the SNR performance loss.

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