Comparison Elements on STG DICE cell for Content-Addressable Memory and Simulation of Single-Event Transients

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Abstract —Comparison elements on base the STG DICE cell and the logical element "Exclusive OR" for a content-addressable memory were designed and simulated. The comparison element contains two identical joint groups of transistors that are spaced on the chip by the distance of four micrometers, so the loss of data in STG DICE cell practically excluded. On the characteristics of the new 65-nm CMOS comparison element, we predict the hardness of these item to single event rate (SER) more to hundred times compared to elements on 6-transistors cells and the standard DICE cell with distances 0.5-0.6 µm between mutually sensitive nodes.

Keywords — content-addressable memory, DICE, logical element, memory cell, single nuclear particle, topology.

I. Introduction

THE feature comparisons in blocks of a content-addressable memory or CAM are realized using combinational logic elements "Exclusive OR" and CMOS 6-transistor memory cells which are used traditionally [1], [2]. The reliability of these memory cells under impacts of single nuclear particles decreased substantially on 65-28 nm bulk CMOS technology.

One of the approaches to the hardened design of CAM is the algorithm of parity-calculating [3], [4], which uses the control of accuracy of the comparison result. The specific error-correcting code was proposed in paper [5] for protecting CAM from multiple cell upsets under impacts of single nuclear particles. The design using replacement of a 6-transistor memory cell on the DICE (Dual Interlocked Storage Cell) with the traditional topology does not solve the problem of the RAM or CAM reliability enhancement [6]. The reduction of distances between pairs of mutually sensitive nodes of the standard DICE cell led to the loss of the resistance to impacts of single nuclear particles [6], [7].

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Experimental studies presented in work [8] demonstrate the high robustness of the 65-nm STG DICE (or Spaced Transistor Groups DICE) compared to the 6-transistor memory cells and standard DICE cells. Transistors are spaced into two groups on topology of STG DICE so that the impact on one group out of two does not cause the failure [9].

II. Schematics of Comparison Elements on STG DICE cell

Fig. 1 demonstrates the scheme of the comparison element, which was designed for CMOS content-addressable memory devices. This unit is based on the STG DICE (Spaced Transistor Groups DICE) with transistors separated into two groups. The STG DICE consists of two groups of transistors $N_D P_A$, $N_A P_B$ and $N_B P_C$, $N_C P_D$ with interleaving pairs of open and closed transistors in each group [9], [10]. In the steady state of STG DICE, the pairs of transistors $N_D P_A$, $N_B P_C$ are closed, and pairs $N_A P_B$, $N_C P_D$ are open if node logic is ABCD = 0101. In the logic of nodes ABCD = 1010 the state of transistor pairs varies.

The combinational part of the logical element in Fig. 1 is the "Exclusive OR" denoted as XOR. Fig. 2 shows two variants of the XOR element: the scheme on two tristate inverters TRInv 1 and TRInv 2 (Fig. 2a) and on two transmission gates TG 1, TG 2 and inverters. (Fig. 2b).

The schemes in Fig. 2a are converted into the scheme in Fig. 2b using the two-wired interconnections of the
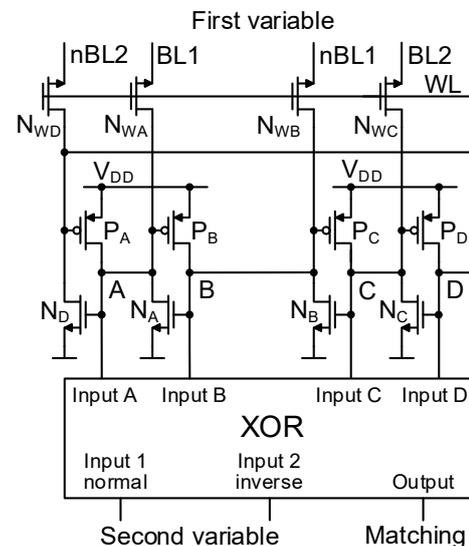

Fig. 1 The scheme of the comparison element on STG DICE cell and the logical element "Exclusive OR".

diffusion scopes located between pairs NMOS and pairs PMOS transistors in Fig. 2a for each of tristate inverters.
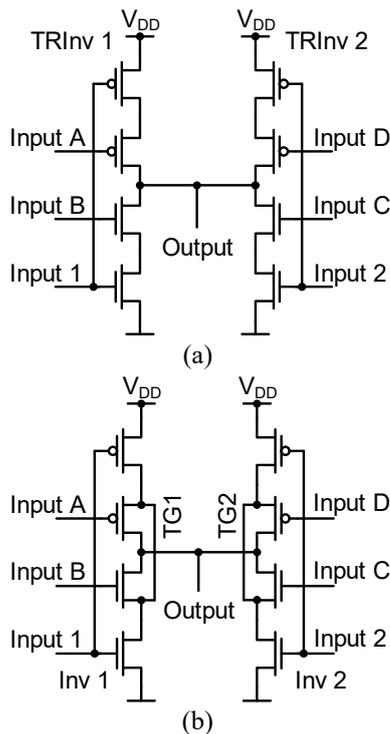

(a)

(b)

Fig. 2 Schemes of the element "Exclusive OR" (XOR): (a) on two tristate inverters TRInv 1 and TRInv 2, (b) on the transmission gates and the inverters Inv. 1, Inv. 2.
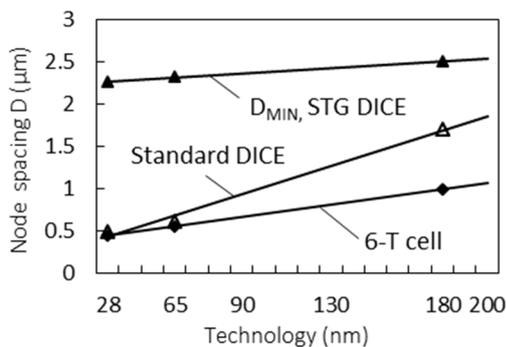

Fig. 3 The minimum distance D_{MIN} for STG DICE and distances D for traditional DICE and 6-T cells as functions of the bulk CMOS technology [11].
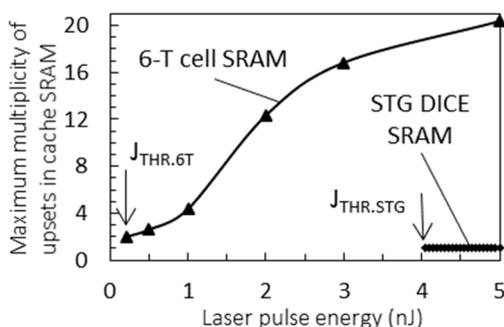

Fig. 4 Maximum multiplicities in 65-nm STG DICE cache RAM 128×32 bit and 6-T cell cache RAM [8].

The comparison element works in two modes. The first one is the recording of one logical variable in STG DICE. Writing of data to STG DICE cell is carried out in four nodes A, B, C, D passing through the gates N_{WA}, N_{WB}, N_{WC}, N_{WD} with bit lines BL1, BL2 in a normal form, and with lines nBL1, nBL2 in an inverse form.

The second mode is the comparison of the first and the second variable. The second variable passes via the Input 1 and Input 2 of XOR (Fig. 2) in the normal and the inverse form. The inverse level may be formed out of the normal using a CMOS inverter.

The logical levels of nodes A and C of STG DICE coincide with the logical level of the first variable, which was written to the cell. Two sequences of the signals in the normal and inverse form reach the inputs of XOR gate synchronously. By comparing these logic levels with the logic of nodes ABCD of STG DICE we get the output of XOR equally the result of comparing (Fig. 1).

The next logical function describes the comparison (matching) data in element XOR during normal steady state STG DICE as:

$$Y_{OUT.XOR} = X_{IN1} \cdot X_{AC} + X_{IN2} \cdot X_{BD},$$

$X_{AC} = X_A = X_C$ are the identical logical levels of nodes A and C, and $X_{BD} = X_B = X_D$ are the identical logical levels of the nodes B and D in the steady state STG DICE cell. $X_{IN1} = X_{CMP}$ is a normal signal at Input 1, $X_{IN2} = nX_{IN1}$ is an inverse signal on Input 2. The results of the comparison from the output of XOR are passed to the matching line.

In the steady state, the logical levels of A and C nodes are identical and the logical levels of B and D nodes are identical. The impact of a nuclear particle on one of the transistor groups inside STG DICE does not lead to a failure, but only leads to a temporary unsteady state [8], [9], and culminates in the return to the original logical state of the nodes after the transition process.

The duration of the time interval of data comparison (matching) is dependent on the duration of the data sequence of the second variable. In this time interval of matching data, it is possible to save the data in the cell if we use the STG DICE instead of 6-T cell or a traditional DICE, where there is a failure of logic due to the impact of single nuclear particles in this case.

III. EFFECTIVENESS OF STG DICE CELL LAYOUT

A. Comparison of STG DICE and traditional DICE Layouts

The minimum distance between mutually sensitive nodes of cells D_{MIN} and the area of the cell are the most important parameters for the estimation of hardness of the DICE design. In Fig. 3are presented the dependences of the minimum distances D_{MIN} between the sensitive nodes of the STG DICE cells with interleaving groups of transistors, the distances D into the standard DICE and 6-T cells as the functions of the technological rules of CMOS design [11].

The minimum distances D_{MIN} for STG DICE depend on design and technological rules (bulk TSMC 28, 65 and 180-nm without the area of guard rings). These parameters obtained by designing the basic memory elements to the cache RAM are on the identical transistors under the same
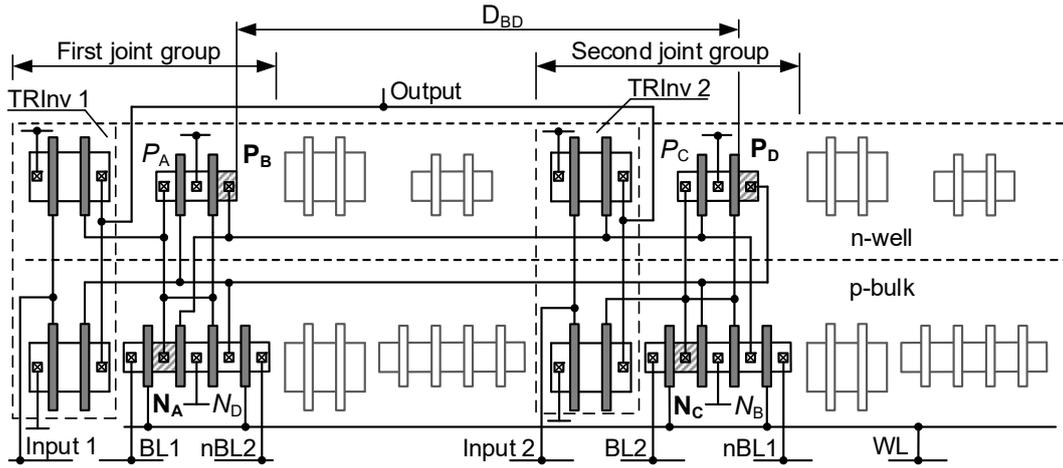
Fig. 5 The layout of the topology of the comparison element on STG DICE and XOR on two tristate inverters TRInv 1 and TRInv 2, D_{BD} = 4.55 μm. The XOR on two transmission gates in Fig. 2b is formed through the additional wired interconnection of the two diffusion regions located between the pairs PMOS and NMOS transistors in each TRInv 1, 2.

technology for the STG and standard DICE. The distances D_{MIN} for STG DICE are within 2.27-2.51 μm, for the DICE reduce from 1.7 μm to 0.5 μm and for the standard 6-T cell are within 1.0-0.35 μm with the norms on reducing from 180 nm up to 28 nm.

The basis of design of memory devices is the requirement that the area of the metallization layer does not exceed the area of the devices layer. Splitting cells onto two groups and interleaving these groups as STG DICE allows creating the spaces between two groups of cells so vast that it would be limited only by an area of the metallization layer of connections inside this basic memory element. That is why the distances between the sensitive nodes in RAM on STG DICE are in the range 2-2.5 μm at 28–180 nm CMOS bulk technology [8].

B. Analysis of Experimental Data

The 65-nm cache CMOS RAM blocks of 128×32 bit on STG DICE cells and 6-T cells were a static cache designed and fabricated using 65-nm bulk TSMC rule [8], [11]. Their resilience was tested using a laser pulse technique.

Fig. 4 shows the dependences of the maximum multiplicities of multi-cell upsets (MCU) as functions of impacts of the laser energy for 65-nm RAM on STG DICE and 6-T cells. The threshold upsets energy for 65-nm STG DICE is $J_{THR.STG}$ = 4.05 nJ and it substantially exceeds the threshold of 6-T cells $J_{THR.6T}$ = 0.8 nJ. The maximum

multiplicity of 6-T RAM is 21 at energy 5 nJ. In contrast to 6-T RAM, MCU are absent in RAM on STG DICE.

IV. LAYOUT OF THE COMPARISON ELEMENT ON TRANSISTORS SEPARATED INTO TWO JOINT GROUPS

To ensure a high level of noise immunity of the comparison element, transistors are separated into two groups that are spaced at a sufficient distance. Fig. 5 illustrates the layout of the topology, where the comparison element consists of two identical joint groups of transistors each contains one group of transistors STG DICE and the one tristate inverter (half of XOR). Two groups of STG DICE are interconnected via two wires only; this minimized the area of a chip. The closed transistors of STG DICE in the nodes state 1010 are marked by bold letters in Fig. 5 and the drains of these transistors are marked hatching. In the other logical state, distances are the same, but between other pairs of nodes, which are marked with italics font in Fig. 5.

The full register contains N comparison elements and 2N joint groups of transistors. In the layout of the register, joint groups are formed as the line in which groups of the same comparison element interleave with joint groups of the adjacent elements. That allows providing the necessary distances between sensitive pairs of transistors in cells.

Table 1 illustrates the distances between pairs of mutually sensitive nodes of the STG DICE memory cell, which belong to different joint groups of one comparison element. These distances are correct in case of interleaving of these groups and the groups of adjacent elements the width of which equals W_{JGR} = 2.4 μm. The minimum distance between the drains of the closed transistors of one cell (table 1) is $D_{MIN} = D_{PB–NC}$ = 4.15 μm.

Table 2 shows the parameters of the joint group on 65 nm CMOS technology, where H_{JGR}, W_{JGR} are the height and width of one joint group of transistors (Fig. 5); I_{LEAK} is the output leakage current of the tristate inverter; $t_{DEL.P}$ is the propagation delay of the XOR element.

The channel widths of NMOS and PMOS transistors of XOR elements are W_N = 300 nm and W_P = 360 nm; the supply voltage V_{DD} = 1 V. The blocks include guard rings around groups of NMOS and PMOS transistors separately

TABLE 1: DISTANCES BETWEEN SENSITIVE PAIRS OF CLOSED TRANSISTORS IN STG DICE CELL

Pairs of nodes	N_A–N_C	P_B–P_D	P_B–N_C	N_A–P_D
Distance (μm)	4.55	4.55	4.15	5.15

TABLE 2: PPARAMETERS OF THE ONE 65 NM CMOS JOINT GROUP OF TRANSISTORS

Parameter	W_{JGR} (μm)	H_{JGR} (μm)	I_{LEAK} (pA)	$t_{DEL.P}$ (ps)
Value	2.4 μm	2.45 μm	30 pA	25 ps

for excluding thyristor effects under impacts of particles. Schematics and topology are designed in CAD Schematics Cadence Virtuoso Editor and Cadence Virtuoso Layout Editor on bulk CMOS TSMC 65-nm technology.

V. EFFECTS OF IMPACTS OF NUCLEAR PARTICLES ON COMPARISON ELEMENTS

According to table 2 the size of one joint group of transistors is 2.4×2.45 μm^2. The direct impact of a single heavy ion on the group of such size will result in collecting lots of induced charges through all reversely biased pn junctions of closed transistors in this joint group. The result will be the distortion of features of the comparison element if as the memory cell is used the traditional 6-transistors cell. This is evident from the experimental data of Multi Cell Upset (MCU) in 6-T RAM with the rule of 65 nm CMOS [12], [13]. This justifies the need of increasing the robustness of logical elements.

The STG DICE cells consist of two groups of transistors so that the impact on one of these groups does not cause the failure [8]. This is based on spacing between sensitive nodes as shown in table 1. STG DICE cells have the high tolerance compared to the 6-transistor memory cells and standard DICE cells.

Accordingly, when the STG DICE cell passes to an unsteady state, through the reverse biased pn junction of transistors of the tristate inverter may flow a pulse of a current from the bulk of the chip. This is the result of the effect of charge collecting from track of a nuclear particle. Using placement of the transistors of one group of STG DICE together with transistors of the corresponding tristate inverter in the joint group, we implement the possibility of the partial correction of changes in logic levels of nodes in a short interval of the unsteady state of STG DICE.

A. The XOR element on two tristate inverters

Tables 3 and 4 demonstrate changes in the logical levels of nodes of STG DICE when the cell is in unsteady state. The output of the XOR with the scheme in Fig. 2a is the result of the combined effects of the changing of Inputs A, B, C, D and the simultaneous impact on transistors of the tristate inverter of this joint group.

In unsteady state of STG DICE, the output of the XOR element takes the high impedance state or the low-level voltage of the output. Table 3 demonstrates results of passing the XOR in high-impedance state after the impact on transistors of STG DICE and changes of logics of its nodes. In this case, both tristate inverters are transferred to the high impedance state of outputs. In table 3, outputs of inverters and the XOR element with the high impedance are marked by the letter Z.

TABLE 3: HIGH-IMPEDANCE STATE OF THE OUTPUTS OF TWO TRISTATE INVERTERS OF THE "XOR" IN THE TRANSIENT STATES OF STG DICE.

Stationary states of STG DICE	"1", ABCD = 1010	"1", ABCD = 1010	"0", ABCD = 0101	"0", ABCD = 0101
Impact on transistors of STG DICE and changes logic on its nodes	on $P_D N_C$ of second group - 1001	on $P_D N_C$ of second group - 1001	on $P_A N_D$ of first group - 1100	on $P_C N_B$ of second group - 0011
Input 1 and Input 2	In1 = 0, In2 = 1	In1 = 1, In2 = 0	In1 = 0, In2 = 1	In1 = 1, In2 = 0
Output of XOR	$Z_1 = Z_2 = Z$	$Z_1 = Z_2 = Z$	$Z_1 = Z_2 = Z$	$Z_1 = Z_2 = Z$

TABLE 4: LOW-LEVEL VOLTAGE OUTPUTS OF TWO TRISTATE INVERTERS OF THE "XOR" IN THE TRANSIENT STATES OF STG DICE

Stationary states of STG DICE	"1", ABCD = 1010	"1", ABCD = 1010	"0", ABCD = 0101	"0", ABCD = 0101
Impact on transistors of STG DICE and changes logic on its nodes	on $P_B N_A$ of first group - 0110	on $P_B N_A$ of first group - 0110	on $P_C N_B$ of second group - 0011	on $P_A N_D$ of first group - 1100
Input 1 and Input 2	In1 = 0, In2 = 1	In1 = 1, In2 = 0	In1 = 0, In2 = 1	In1 = 1, In2 = 0
Output of tristate invertor TRInv 1	$Z \to 1 \to 0$	$Z \to 0 \to 1$	1	0
Output of tristate invertor TRInv 2	0	1	0	1
XOR output $b \times V_{DD}$, b = 0.17	$b\downarrow$	$b\uparrow$	$b\uparrow$	$b\uparrow$
Simultaneously impact on the invertor corresponding the group	on $NMOS$ of Inv. 1	on $PMOS$ of Inv. 1	on $PMOS$ of Inv. 2	on $PMOS$ of Inv. 1
The effect of simultaneous impact on the tristate inverter	correction the logic output level	correction the logic output level	correction the logic output level	worsens the logical level of output
Examples of curves in Figs.	Fig. 6a	Fig. 6b	Fig. 7a	Fig. 7b

TABLE 5: LOW-LEVEL VOLTAGE OUTPUT OF THE "XOR" ON THE TRANSMISSION GATES IN THE TRANSIENT STATES OF STG DICE

Stationary states of STG DICE	"0", ABCD = 0101	"0", ABCD = 0101	"0", ABCD = 0101	"0", ABCD = 0101	"1", ABCD = 1010	"1", ABCD = 1010
Impact on transistors of STG DICE and changes logic on its nodes	on $P_A N_D$ of first group - 1100	on $P_A N_D$ of first group - 1100	on $P_C N_B$ of second group - 0011	on $P_C N_B$ of second group - 0011	on $P_B N_A$ of first group - 0110	on $P_B N_A$ of first group - 0110
Input 1 and Input 2	In1 = 0, In2 = 1	In1 = 1, In2 = 0	In1 = 0, In2 = 1	In1 = 1, In2 = 0	In1 = 0, In2 = 1	In1 = 1, In2 = 0
Values of the coefficient b	0.5	0.17	0.17	0.5	0.27	0.27
XOR's output V_{OUT}, V	0.5	0.17	0.17	0.5	0.27	0.27
The effect of the impact through STG DICE to the output of XOR	Output level is undetermined	Output level is proper	Output level is incorrect	Output level is undetermined	Output level is proper	Output level is incorrect

Table 4 demonstrates results of transition of the XOR output to the low-level voltage state after the impact on STG DICE. In this case, the output of one inverter TRInv is in the state "0" and the other item is in "1". This is the result of changing logical state of two nodes in STG DICE. In this case, the voltage output is $V_{DD} \times b = 170$ mV. The value of the factor b depends on the ratio of widths of NMOS and PMOS transistors in XOR. The low-level voltage output when $b = 0.17$ means the logical output level $Y_{OUT.XOR} = $ "0".

When transistors of the tristate inverter are located near the corresponding group of STG DICE, the simultaneous impact of a charge on STG DICE and the closed transistor of the tristate inverter may give the effect of correction or deterioration of the logical level of output. Vertical arrows near the coefficients b↑ or b↓ in table 4 indicate the direction of the changing of the output voltage due to the simultaneous impact of the current pulse through the pn junction of the closed transistor of the tristate inverter.

The changes of the pair of inputs of XOR during unsteady state of STG DICE were simulated using voltage pulses with the amplitudes equal to V_{DD} and duration at 120 ps. The modeling of the charge collection in tristate inverters was using the current pulses as

$$I(t) = (Q_{COLL.XOR}/(\tau_F - \tau_R)) \times (\exp(t/\tau_F) - \exp(t/\tau_R)).$$

The rise time and the fall time constants are $\tau_R = 5$ ps and $\tau_F = 50$ ps, the collected charge is $Q_{COLL.XOR} = 7$ fC.

Figs. 6 and 7 present the voltages on STG DICE nodes A, B, C, D and the output voltage of XOR during the time of an additional impact of a current pulse through the reverse biased pn junction of inverter TRInv 1 or TRInv 2. These dependencies are for the two expected values of XOR output as logical "0" (Fig. 6a) and logical "1" (Fig. 6b). These two impacts are described in table 4 under marking "example in Fig. 6a" and Fig. 6b. The beginning of pulses is at time 200 ps, the end is at time 320 ps.

The simultaneous impacts of the charge on one group of transistors STG DICE and the current pulse through the reverse biased pn junction of the corresponding TRInv 1 (Fig. 6) indicate the correcting of the two wrong comparison results. Fig. 6a demonstrates the example of the correction by decreasing the logical level "0". Fig. 6b presents the correction of the output level through raising from the wrong level "0" up to "1".

Fig. 7 presents two examples for the expected logical "1" (Fig. 7a) and logical "0" (Fig. 7b) for XOR outputs in case of the initial state of STG DICE ABCD = 0101. These two impacts are described in table 4 under marking correction by raising the wrong level "0" up to "1". Fig. 7b presents the wrong raising of the logical level of output from the right level "0" to the wrong level "1".

(a)   (b)
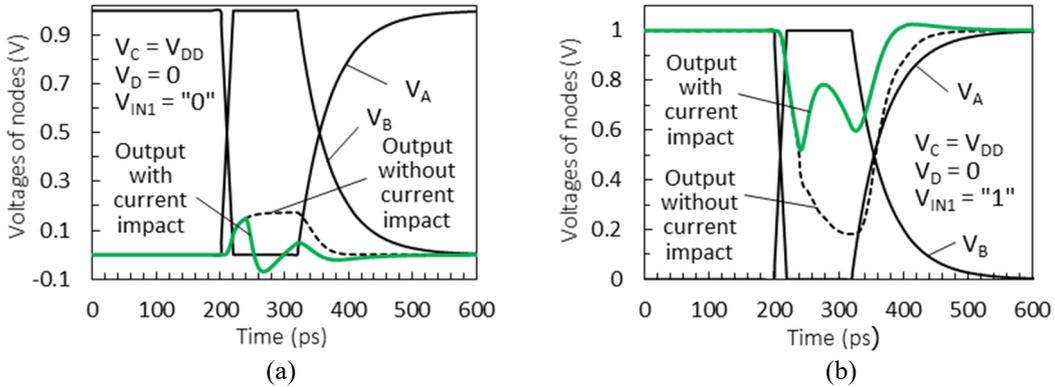
Fig. 6 The nodes voltages relative to the time of transition of STG DICE from the steady **1010** to unsteady state 0110 and the return. The correction of the output XOR is by the additional impact of a current pulse through the inverse bias pn junction of TRInv 1: (a) Input 1 is "0" and Input 2 is "1"; (b) Input 1 is "1" and Input 2 is "0".
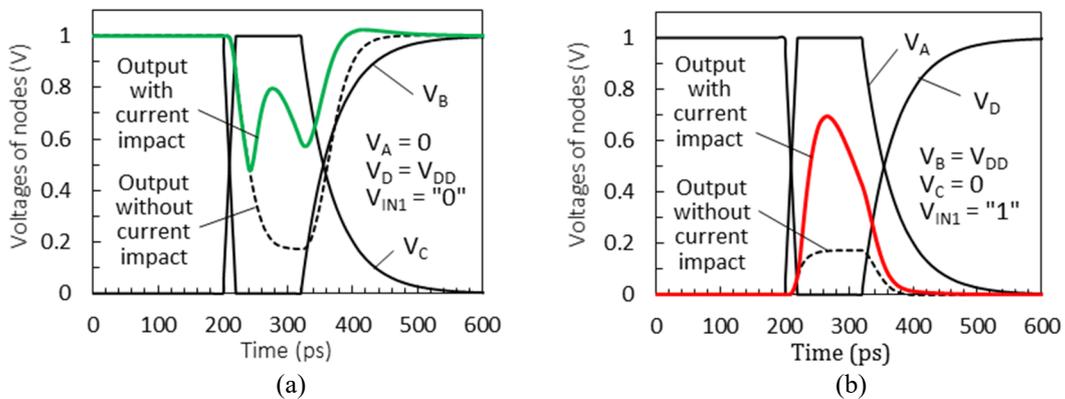

(a)   (b)

Fig. 7 The nodes voltages relative to the time of transition of STG DICE from the steady **0101**: (a) to unsteady state 0011 and the return, Input 1 is "0" and Input 2 is "1"; (b) to unsteady state 1100, Input 1 is "1" and Input 2 is "0". The correction of the output XOR is by the additional impact of a current pulse through the pn junction of the second TRInv 2 (in case Fig. 7a) and the worsening of the output level in case of the impact on the first TRInv 1 (Fig. 7b).

The dashed curves in Figs. 6 and 7 correspond with the output voltages of XOR element without the influence of the additional impacts of current pulses. The solid-line curves correspond with the additional impact of the current pulse on TRInv 1 or TRInv 2 during unsteady states of STG DICE cell. Co-location transistors in two joint groups give the possibility of the correction of the comparison error when STG DICE is in unsteady state.

B. The XOR element on two transmission gates

Table 5 demonstrates the feature of the XOR element on two transmission gates with the scheme in Fig. 2b. The comparison element on this XOR element may be in one of the eight unsteady states of STG DICE under the impacts of single nuclear particles. The XOR element in two cases passes in a high-impedance state at its output. In six other cases (table 5), in unsteady state of STG DICE the output voltage of comparison element has the values $V_{OUT} = b \times V_{DD}$, where factor $b = 0.17; 0.27; 0.5$ depending on the specific unsteady state.

Fig. 8 shows the example of the output voltage of the XOR element in time for the case when $b = 0.27$ for the correct logical output level that equals "0". In table 5 all six variants vary only by the factor of the division voltage b depending on the number of open transistors in the gates TG1, TG2 and the inverters Inv 1, Inv 2 in the specific unsteady state.

This XOR element under impacts of particles in two from six cases of unsteady states will have the proper output levels (table 5), in two cases it will have incorrect output levels and in two cases output levels will be undetermined ($b = 0.5$).

The simulation has shown that efficient correction of the output signals is impossible in this type of comparison element. The impact of the current pulse on the closed transistors of XOR in unsteady states of STG DICE does not lead to better recovery of the proper result of the comparisons than in XOR on base tristate inverters.

The simulation of effects of changing voltages on output of XOR demonstrates the problems of designing hardened CMOS elements for a content-addressable memory. More research is needed on the effectiveness of the topology options to minimize the effects of particles.
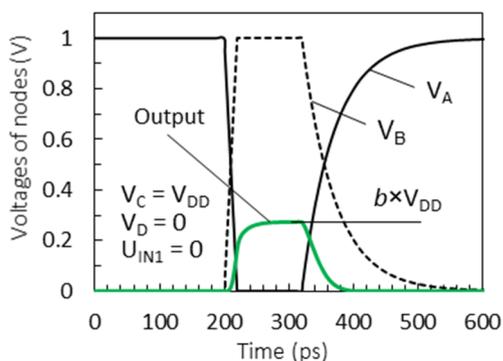

Fig. 8 The voltages on the output XOR and nodes STG DICE during transition from the steady 1010 to the unsteady state 0110, Input 1 is "0", Input 2 is "1".

VI. CONCLUSION

The comparison elements were presented for a content-addressable memory as elements with the new topology with the separation of transistors into two identical groups. This design provides large spacing between mutually sensitive nodes of the memory cell and may implement the correction of the comparison error when STG DICE cell is in an unsteady state. The best version is the element based on the XOR on two tristate inverters. The proposed methodology is promising for design of nanoscale elements for microprocessor systems with increased resistance to impacts of single nuclear particles.

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